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Additional inventors are being named on the 1 *separately numbered sheets attached hereto*

TITLE OF THE INVENTION (500 characters max)

COLOUR SENSORS BASED ON (J)FET STRUCTURES

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[Page 1 of 2]

Respectfully submitted

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Date February 17, 2004

REGISTRATION NO. 26,868 *(if appropriate)*

Docket Number: 1461/8 PR6

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Number 1 of 1

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PROVISIONAL APPLICATION

FOR

UNITED STATES LETTERS PATENT

TITLE: COLOUR SENSORS BASED ON (J)FET STRUCTURES

APPLICANT: Daniel Puiu POENAR and Mihaela CARP

JFET- & Multijunction-based Colour Sensors
Literature review, Theoretical background, Patent search

1. Basic principles of colour sensing

1.1- WHY?

Optical and colour monitoring is essential in many medicine and biology-related applications. In such cases, absorption/transmission in the visible range through the studied cells/tissue is used, and colour sensors are thus necessary for a correct reading. This colorimetric approach is particularly important in medicine and biology as colour often is an indicator of state of health and it is also used for cell and tissue analysis. For instance, simple typical applications are colour reflectance photometers that can detect changes in the colours of an array of special substances that are used for medical analyses (such as blood and urine analysis) [1]. A distinctive place is devoted to hemoglobin measurements that are carried out almost exclusively using such optical methods. Transmission or reflectance methods can be employed to determine the blood oxygen content, and both of them rely on the differences between the absorption coefficients of oxy- and deoxy-hemoglobin. The oxygen saturation, SaO_2, is defined as the ratio between the concentration of oxygen-carrying hemoglobin (= oxyhemoglobin) and the total sum of oxyhemoglobin and deoxyhemoglobin present in the blood stream:

$$SaO_2 = \frac{c_{OX}}{c_{OX} + c_{DOX}} = \frac{c_{OX}}{c_{Hb}} \qquad (1)$$

Assuming blood plasma to be transparent, the attenuation coefficient μ_i can be written as:

$$\mu_i = a_{i,OX} c_{OX} l_{i,OX} + a_{i,DOX} c_{DOX} l_{i,DOX} + S_{i,SaO2,Hct} \qquad (2)$$

where a= absorption coefficient, l= optical path length and $S_{i,SaO2,Hct}$= scattering component dependent on wavelength, O_2 saturation and hematocrit values, respectively, whereas subscript i describes the wavelength and subscripts OX & DOX refer to oxyhemoglobin and deoxyhemoglobin, respectively. Knowledge of the extinction coefficients at two suitable wavelengths and of the influence of scattering by blood cells enables the calculation of c_{OX} and c_{DOX}, from which SaO_2 and c_{Hb} are subsequently computed. A practical realization performed the measurements at 660 and 950 nm, respectively, and the red and IR LEDs were modulated with different frequencies (500 and 700 Hz, respectively) [2].

However, the reflection methods apparently may overcome some drawbacks of the transmission (low optical density & non-linearity). Moreover, for a microfabricated device a transmission measurement is more feasible than a reflectivity one.

Besides medicine and biology, colour measurement is important in food industry, as well as in the printing or cosmetics industries. In the food industry colour can be used either for quality estimation, or for automatic selection of products in different categories. Fig.1-a shows the reflectance spectra of beef meat and their variation in time. Even if the measurement was performed at a very low temperature (to estimate the degradation of meat under storage conditions), it is quite clear that the typical spectrum changes in time due to exposure to oxygen, which causes the oxymyoglobin to be oxidized into methemyoglobin. Similar colour-based quality analysis (for diagnosis of storage conservation or for estimation of their alimentary properties) can also be performed on other foods as well, e.g. milk, orange or strawberry juice, or peach nectar [3]. Fig.1-b shows how the quality decrease of orange juice due to water dilution can be easily estimated using such colour spectra. Of course, particularly for such liquid samples, the transmission method is again much more appropriate and thus the most often employed.

In conclusion, it is important to realize and employ good colour detectors as they allow to quantize in measurable units the optical changes that appear in the transmission of the substance or cell which they analyze.

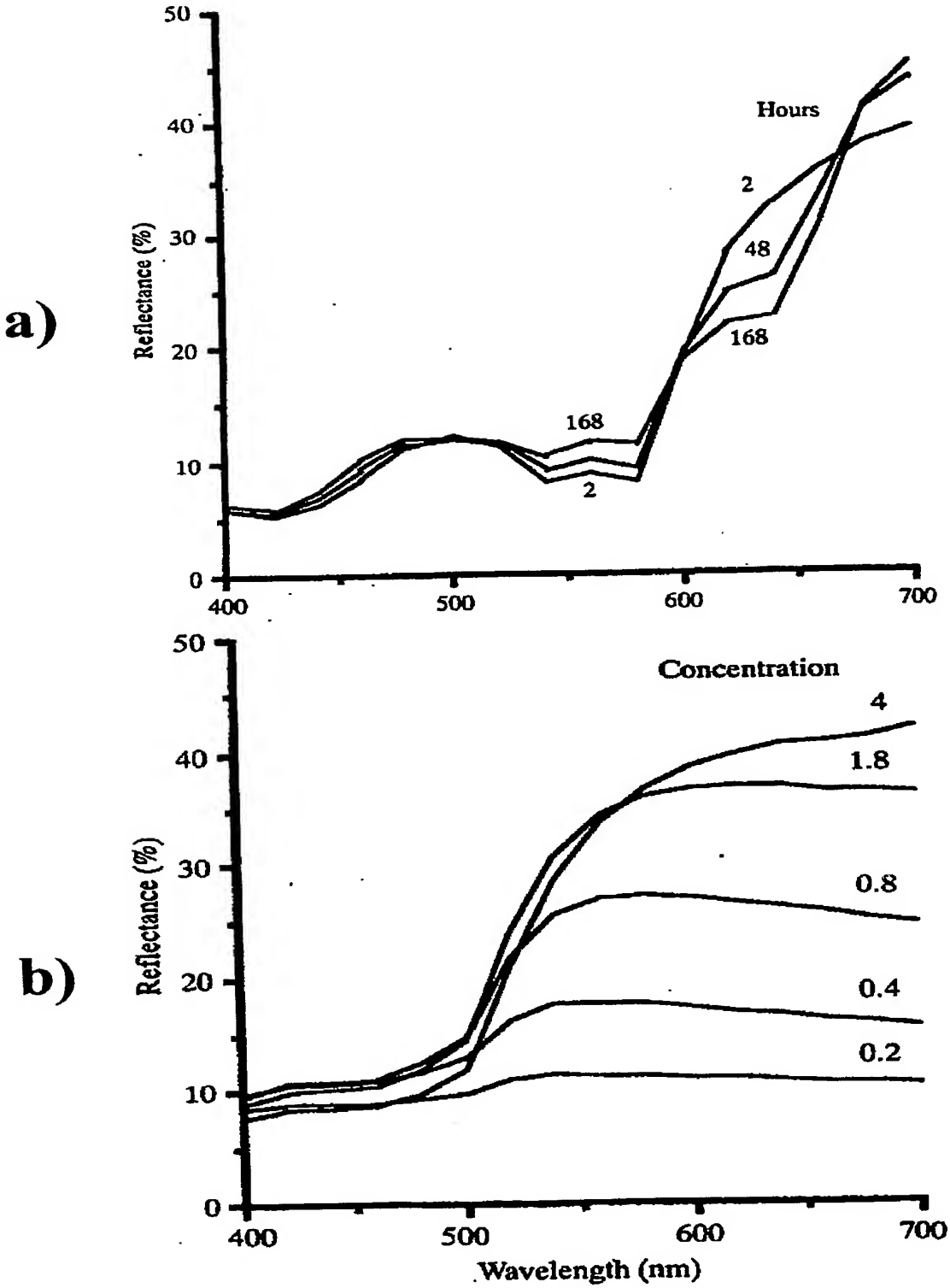


Fig.1: a) Reflectance spectra of fresh beef, calculated as average over more than 100 samples wrapped in oxygen-permeable film and stored at <5°C under 1000 lux fluorescent illumination for the number of hours stated on the corresponding curves;
b) Reflectance spectra of concentrated and diluted orange juice at a path length of 4 cm. Normal juice concentration =1; the higher number was obtained using juice concentrate [3].

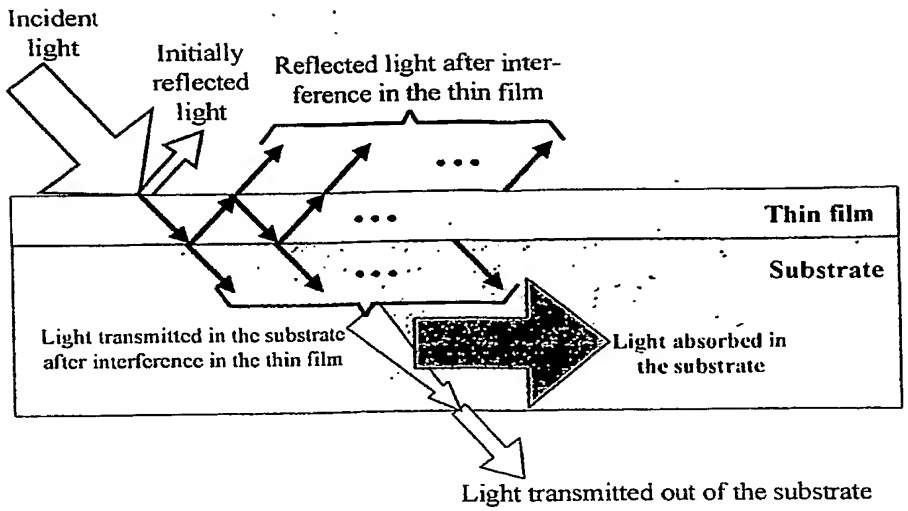


Fig.2: Reflection, interference, transmittance and absorption of light for a system comprised of a transparent thin film deposited on an absorbing substrate.

1.2- HOW?

1.2.1- Optical properties of semiconductors

Fig.2 shows the general case for the interaction of light with a solid–state system composed of a substrate covered with a top coating. Reflection of light waves occurs whenever the light penetrates from one medium into another, the reflected amplitude being dependent on the differences in refractive indices between the two materials at each specific wavelength. Therefore, when light is incident on a transparent thin film it produces two reflected beams: one from the front and one from the back surface. These two beams can interfere with each other to enhance or reduce the light intensity. However, for understanding the operation of a photodetector is more important to highlight another important optical phenomenon, namely **absorption**.

In vacuum the speed of light $c = 3 \times 10^8$ m/s but in any medium the speed of light c_m is smaller

$$c_m = \frac{c}{n} \qquad (3)$$

where n_r is called refractive index. Accurate description of optical phenomena require, however, the usage of the so-called "characteristic (optical) admittance" of a medium, $N=n-ik$, which is typically referred to as the "complex refractive index" (although this denomination is a misnomer, due to the definition of a refractive index as the ratio between two real numbers, i.e. velocities). Its two components are n=the refractive index, and k= the extinction coefficient (related to losses, i.e. the attenuation of light propagating through the respective material), respectively. Both n and k are material properties [4]:

$$n^2 - k^2 = \frac{\varepsilon_r}{\mu_r} \qquad (4), \quad \text{and} \quad 2nk = \frac{\mu_r \sigma}{\omega \cdot \varepsilon_0} \qquad (5)$$

where ε_r and μ_r are the relative permittivity and permeability of the material, σ the electric conductivity of the material, ε_0 the permittivity of vacuum and ω the angular frequency of the electromagnetic wave. Finally, it must be highlighted that in any material, both n and k are varying with the wavelength, $n = n(\lambda)$, and $k = k(\lambda)$.

Based on k, one can define the so-called absorption coefficient α as:

$$\alpha = \frac{4\pi k}{\lambda} \qquad (6)$$

This means that the attenuation of light after traveling through a sheet of material of thickness "x" will be $\exp(-\alpha x)$.

As mentioned before, k is wavelength dependent. Fig.3 shows that in silicon, k decreases significantly (quasi-exponentially) with the wavelength [5]. Therefore, by calculating the attenuation of light based on eqn.(6), one can immediately realize that incident light of different wavelengths will have different penetration depths in the medium (silicon), i.e. the longer the wavelength, the deeper the penetration depth (i.e. the distance at which the light intensity decreases, e.g. 'e' times, where e=2.71..., the base of the natural logarithm, although it would be more practical to calculate a decrease with an order of magnitude in light intensity for the desired wavelength). The direct consequence of this fact is much more vividly depicted in Fig.4: the violet-blue hues (short wavelengths) of the visible range will be extremely quickly and efficiently absorbed in an extremely thin layer situated at the top-most of the silicon substrate. As light advances deeper in silicon, the longer wavelengths, green and yellow begin to be absorbed, though not as well as the shorter ones, so that these colours are absorbed only mildly at a greater depth (1...3 μm from the surface). Finally, k has the smallest values for the longest wavelengths, which means that the red hues are only slightly absorbed in Si and at great depths (>5 μm), meaning that the detection of this colour requires a very wide detecting region deeply situated within the Si structure. If a normal Si substrate is used (650 μm thick), then all light will be absorbed within the wafer and no transmitted component will appear.

Hence, the dependence of k on λ is one fundamental principle on the basis of which colour sensors are constructed.

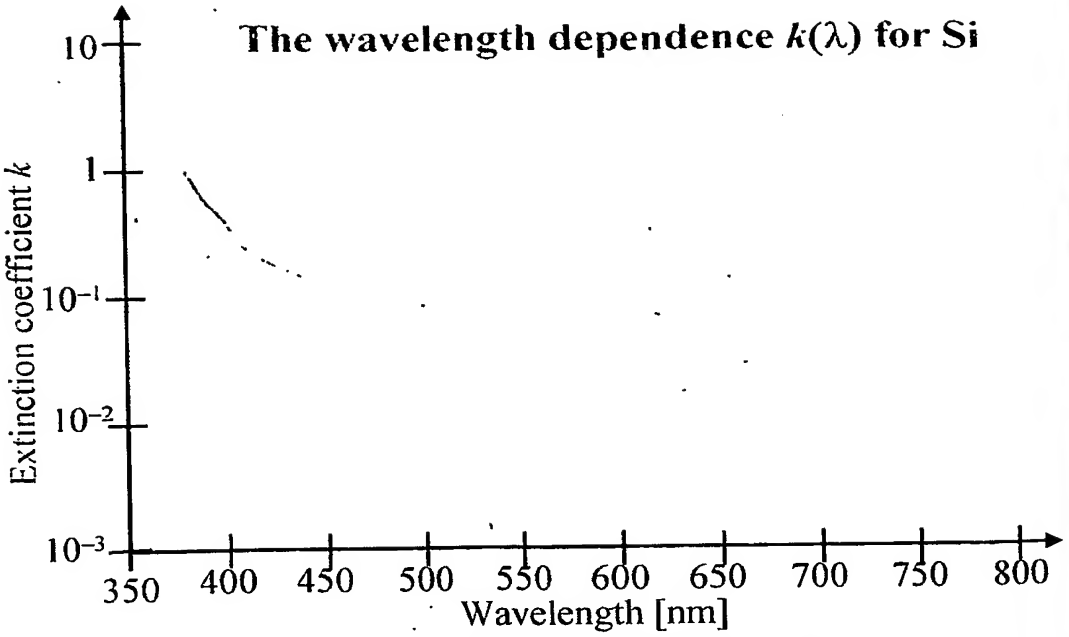


Fig.3: The wavelength dependence of the silicon's extinction coefficient k [5].

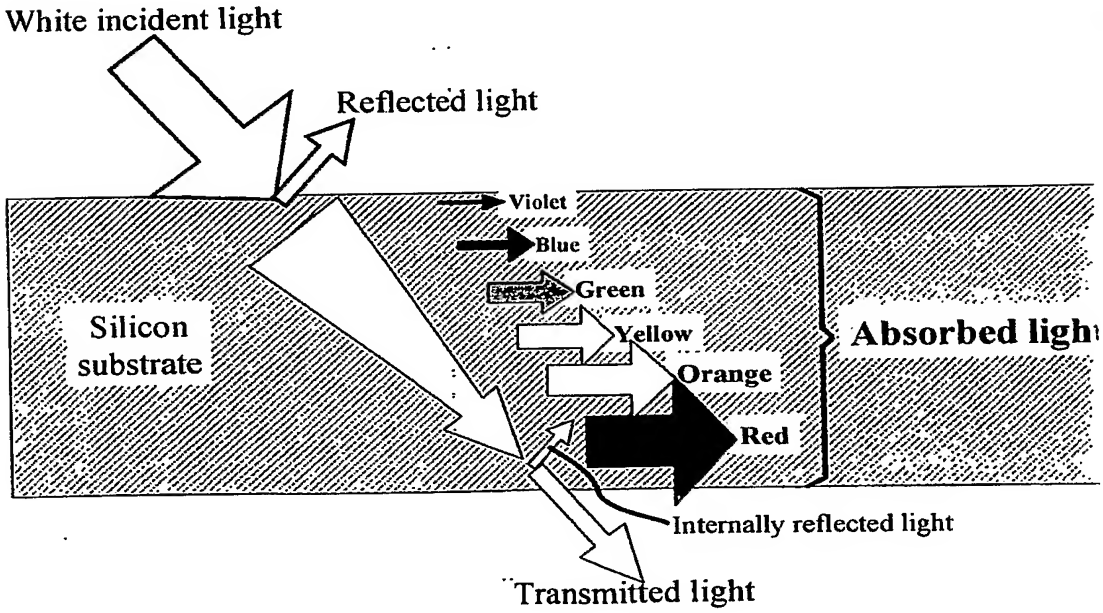


Fig.4: Light incident on a semiconductor penetrates through it selectively, with various wavelengths absorbed differently at different depths. The widths of the horizontal arrows (signifying the portions of absorbed light) are -in a non-exact quantitative but illustrative qualitative manner- directly proportional with the widths of the detection regions necessary in order to absorb each specific radiation, while at the same time being inversely proportional with the absorption efficiency of that wavelength.

1.2.2- The simplest light detector: the photodiode

Let's address quickly the other important solid-state phenomenon important for the operation of any semiconductor-based optical detector: photogeneration.

Photons are absorbed in a solid through a process known as the ***photoelectric effect*** whereby *a photon interacts with an electron by giving all its energy to the electron. In effect, the photon disappears and its energy is transferred to an electron.* The photoelectric process is responsible for the absorption of visible-light with energies of 2 to 3 eV as well as for X-rays with energies a thousand times greater than that of visible light. The energy can be high enough th make an electron reach the valence band and become a free carrier. An intrinsic semiconductor uses such band-to-band transitions, responding to radiation with wavelengths $\lambda(\mu m) < 1.24/E_g\ (eV)$ where E_g is the semiconductor's energy gap. Intrinsic semiconductors may often operate at cryogenic temperatures, since at higher temperatures their conductivity may be dominated by carriers thermally excited from impurity levels. However, the largest part of the practical applications typically use extrinsic (i.e. doped) semiconductors, like Si.

For a uniform illumination, the generation rate of electron-hole pairs is given by $G_L(\omega)=\frac{Q_C P_I}{\eta\omega L}$ where P_I is the absorbed optical power per unit area (in W/m^2), L is the active thickness of the photoconductive film, and Q_C is the quantum efficiency, i.e. the number of electron-hole pairs created per absorbed photon.

Depending on whether the semiconductor is intrinsic or extrinsic, the absorption of light quanta –photons–may cause different types of transitions that increase the concentration of electrons in the conduction band and/or holes in the valence band, as it is schematically shown in Fig.5. However, the carriers once generated and set free also induce a second important effect, namely ***photoconductivity***, i.e. *the modulation of (or inducing) the semiconductor's electrical conductivity due to the addition of free carriers generated by the absorption of photon energy.* The rate at which free electrons are generated and the time they over which the remain free determines the amount of the increase. This effect is most important if photogeneration takes place in either an extrinsic or a neutral semiconductor (*n*- or *p*-type). However, the greatest majority of semiconductor devices (like the photodiode, the phototransistor and the CCD structure) employ photogeneration in a depleted region. Fig.6 shows the photogeneration in a *p-n* junction. The junction will always exhibit a depleted region right at the junction between the two neutral regions. This depletion region has a built-in electric field caused by the fixed space charges generated due to the initial diffusions of majority carriers across the junction. If a photon falls unto this region, the carriers thus photogenerated will be immediately separated by this internal electric field and will drift towards the respective regions where they are majoritary: the electrons towards the *n*-region, and the holes towards the *p*-region, respectively. Obviously, the wider the depleted region (i.e. the stronger the externally applied reverse bias), the larger the number of photogenerated carriers, and hence the detected photocurrent. Of course, photogeneration can still occur in the neutral regions as well (provided that they are exposed to the radiation), but from these carriers only the minority ones who can diffuse up to the edge of the depleted region will contribute to the overall photocurrent. Consequently, if the neutral region is too wide, the diffusion current toward the depleted region is significantly impeded and the detected photocurrent is low. Thus, for a large photoresponse signal a high reverse bias should be applied as to widen as much as possible the depleted region. At the same time, the higher internal electric field will not only widen the depleted region but will also help in a very quick transition of the carriers across the depleted regions, towards the narrowed neutral regions, and then through the contacts towards the external circuitry. The depleted region and its internal electric field therefore become extremely important to photodiode performance as they provide the faster portion of device response and convert the incident photons into electron-hole pairs at higher efficiency.

A large number of optical sensors rely on the operation of one, or more, *pn* junction(s): the photodiode, the phototransistor and the photothyristor. All the devices to be detailed in the next section employ the same principle: detection of light using the photogeneration within a depleted region at a *pn* junction. However, there also exist other types of photodetectors, such as the CCDs, which rely on using MOS structures. Nevertheless, they still employ the same principle, i.e. photogeneration within a depleted region, only that this depleted region is now generated using a MOS

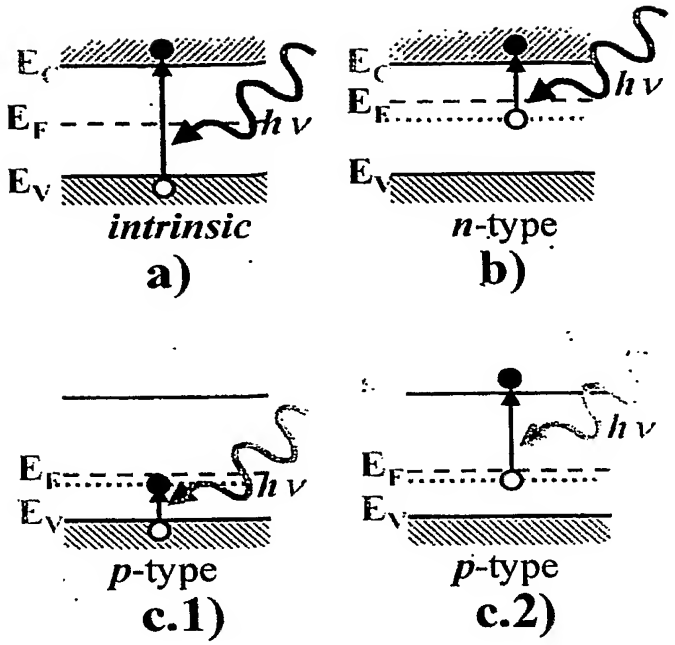


Fig.5: Energetic transitions caused by photon absorption in semiconductors: (a) in an intrinsic semiconductor (valence band to conduction band transition), (b) in an extrinsic semiconductor (transition from a deep donor level to the conduction band), (c1) and (c2): also in an extrinsic semiconductor, first a transition from a the valence band to a deep acceptor, and then from the deep acceptor level to the conduction band.

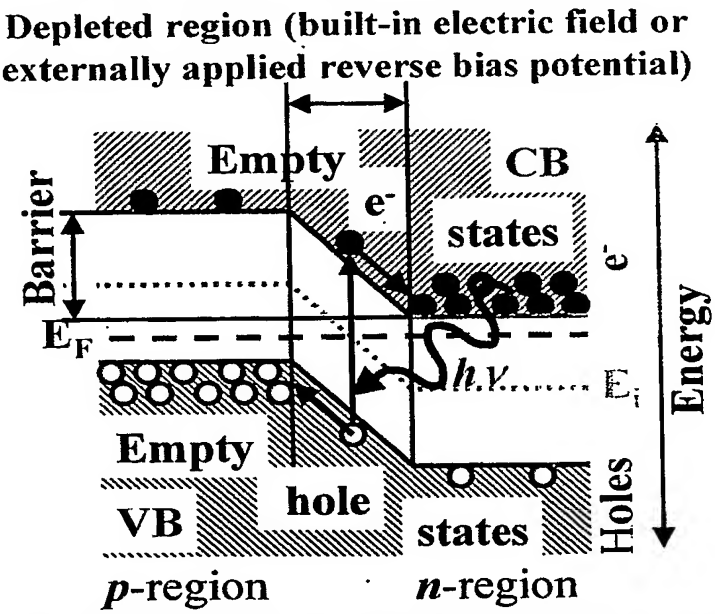


Fig.6: Band diagram of a photodiode under zero/reverse bias and the photocurrent generation.

structure. This allows not only achieving significant integration levels at small sizes, but also allows for convenient trasportation of the photogenerated charges by wisely manipulating the potentials applied unto cascaded MOS cells.

Finally, another type of photodectors may rely exclusively on photoconductivity effects, resulting in extremely simple and cheap devices.

1.2.3- Colour sensing

A pragmatic way to conceive a colour sensor (especially for practical real-life imaging applications) is to fabricate it as an array of cells comprising three independent photosensors, each of them detecting only one primary colour. Therefore, the easiest implementation of such colour sensors uses coloured filters obtained by depositing different polymer dyes on top of the photosensors [6]. Knowing the transmittance characteristics of the polymer dyes and the photocurrent output of each of the three photodiode elements, it is possible to calculate the unique position of the colour of the incident light. However, this *classical approach* of realizing a colour sensor has two important *disadvantages*:

1) It employs polymer dyes as colour filters.

This can lead to inherent variations in the colour selectivity of the filters, and/or incompatibility with other technological steps, especially when smart sensors are desired to be realized. (For instance, when such filters must be implemented in systems that have to be processed using bulk micromachining techniques, the polymer dye is inconvenient to be deposited before the KOH etching and it is impossible to spin it on the wafer after the microstructures are formed).

2) Two or three photodiodes are necessary for each element, (this leads to a large area occuppied by one entire pixel).

The first disadvantage can be eliminated by replacing the polymer layers with interference filters that can be realized using materials compatible with the standard Si-processing. Furthermore, the design flexibility is improved because the structure of the filter can now be designed to meet any imposed requirements, not only those dictated by the used polymer. This technique, combined with a careful control of the doping profile of the photodetector in the substrate was successfully used to fabricate sensors with any desired spectral response [7].

Fig.7 shows the classical configurations used in typical photodetectors.

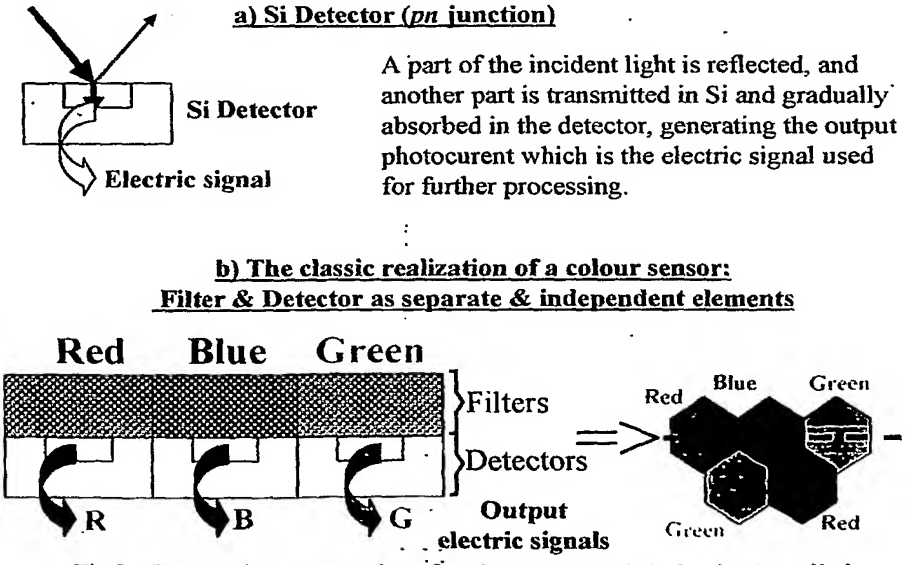


Fig.7: Classical implementation of optical sensors: a) A simple photodiode, b) The principle used for typical colour detection.

However, a complete colour-sensing cell would still require more than one photodiode, and the replacement of the coloured polymers with interference filters may improve the filtering performance but provides neither additional signal processing flexibility nor a more compact sensor. Therefore, different implementation approaches are required to obtain both increased flexibility in controlling the spectral response signals and complete colour detection with only one single sensing element. In principle, two techniques can be used to meet these requirements:

A) Reverse-bias scanning of a junction.

This method is based on the dependence of the extinction coefficient k (the imaginary part of the complex refractive index, $\mathbf{N} = \mathbf{n}-i\boldsymbol{k}$) on the wavelength λ. As presented previously, this phenomenon, called dispersion, is present for any material, for both **n** and k, and Si presents a strong dispersion of k. Because photons of different wavelengths are absorbed in Si at different depths one can obtain an adjustable confinement of the depth in Si in which penetrating photons can contribute to the photocurrent by placing various junctions at different depths, with a controllable width of the depleted region of each junction. The effect can be used either to obtain a sensor made up of two diodes with depletion widths of different values that provide information about the "average colour" of the light [8], or to fabricate a sensor having the central wavelength of the response electronically tunable by varying the reverse voltage applied across the photodiode [9]. In this latter case (schematically presented in Fig.8), only one single diode is required for each colour element and a size reduction for the colour imaging sensor is thus achieved.

B) Vertical stacking of several detecting junctions.

In this case, the detectors are placed not horizontally but integrated in a vertical structure. A simple sensor of this type has been constructed for monitoring the colour of a combustion flame, and it comprised of a dual photodiode structure monolithically integrated in a *pnp* vertical structure as shown in Fig.9, where both the schematic cross-section (a) as well as the equivalent circuit (b) of the device are presented. The short-circuit current ratio of the two photodiodes varied monotonically with the wavelength in the range 400...1000 nm and also cancelled out the influences of adverse effects such as temperature and contamination of the optical window of the sensor [10].

The next step is to add flexibility to the control of the spectral responses of this dual-junction structure. Because the photocurrent detected in the upper or lower junction is due to contribution of several wavelength ranges, spectral response shaping techniques can be achieved by selective omission or supply of these components to the detected photocurrent in one of the junctions. Increasing the collecting depth down from the upper junction will favor the long-wavelength response of this junction, whereas an increase of the lower junction's depletion region will improve the short-wavelength response of the lower junction at the expense of the long-wavelength response of the upper junction. This realization is entirely compatible with standard processing and allows electronic tuning of the spectral response, but it provides only two colour signals [11].

Therefore, three junctions should be used for photodetection in order to obtain a complete colour sensor that would provide signals for all the three primary colours. Fig.10 shows the structure of such a sensor with three vertically integrated photodiodes. Its functioning relies on the dispersion of k with λ so that the thickness of the silicon itself serves as a natural spectral filter. The optimum responses are achieved when the depletion region of the top diode extends in depth between 50 and 200 nm from the surface, the middle depletion region extends from 200 to 800 nm, and the lower depletion region should extend from 1500 to 500 nm (the substrate-epi junction is not used). The structure has been implemented using a Selective Epitaxial Growth (SEG) process, which enables selective stacking of additional epitaxial layers after completion of the conventional processing. Its fabrication is compatible with the standard bipolar processing and enables on-chip integration of read-out circuitry to realize a smart sensor on a single chip [12].

Similarly complex devices, such as thyristor-type *pnpn* structures, can also be employed for simultaneous detection of the three primary colours [13]. Such an approach has been started and developed in the "Biochemical Sensing Devices" Project (RG00/11, started on 20 Dec.2000) by the Principal Investigator (Assist.Prof. Poenar Daniel Puiu) with one of his Ph.D. students, Mr. Chen Jun. Fig.s 11-a, -b and –c show the schematic cross-sectional structures for an ideal device of this type and for the two practical versions proposed for actual implementation, respectively, whereas Fig.12 shows

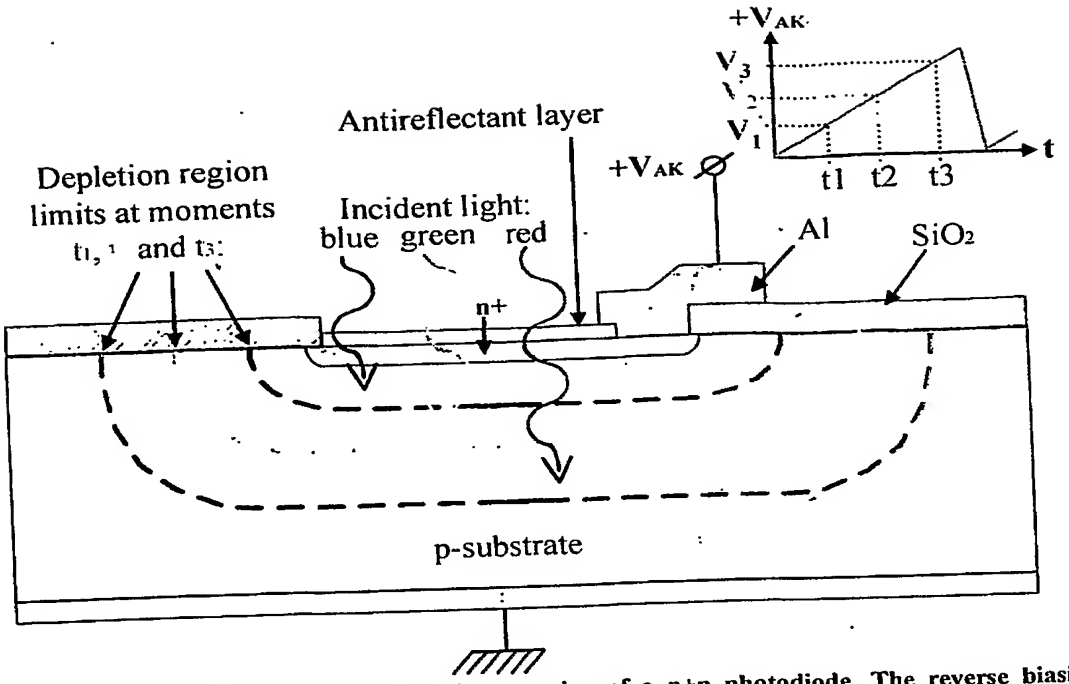


Fig.8: Colour detection by reverse-bias scanning of a n+p photodiode. The reverse biasing voltage varies in time, resulting in width variations of the depletion region which will thus collect successively the carriers photogenerated by incident light of different wavelengths [9].

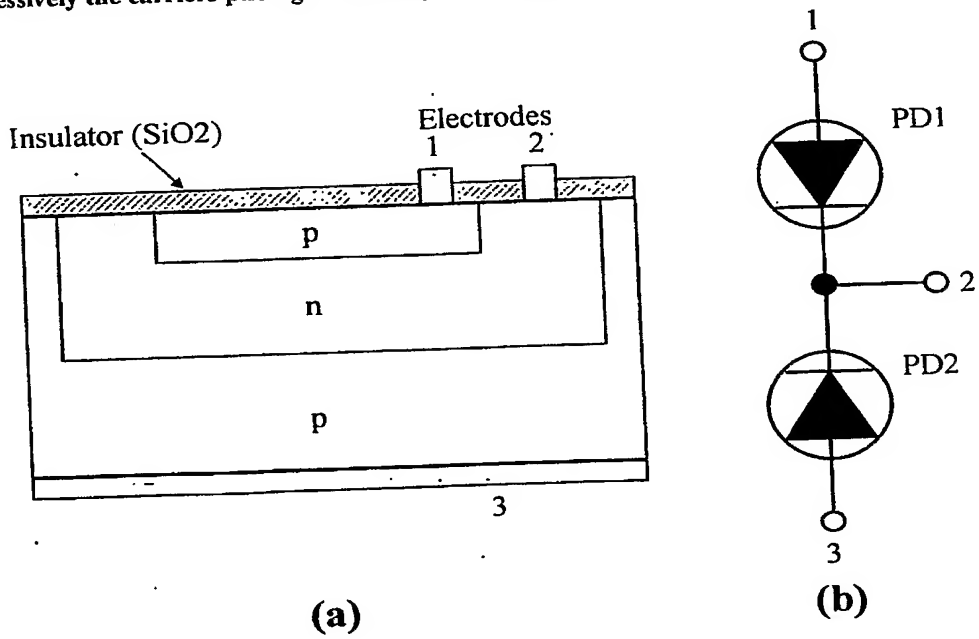


Fig.9: Simple colour sensor with vertically-stacked junctions: (a) Schematic cross-section; (b) Equivalent circuit [4. 8].

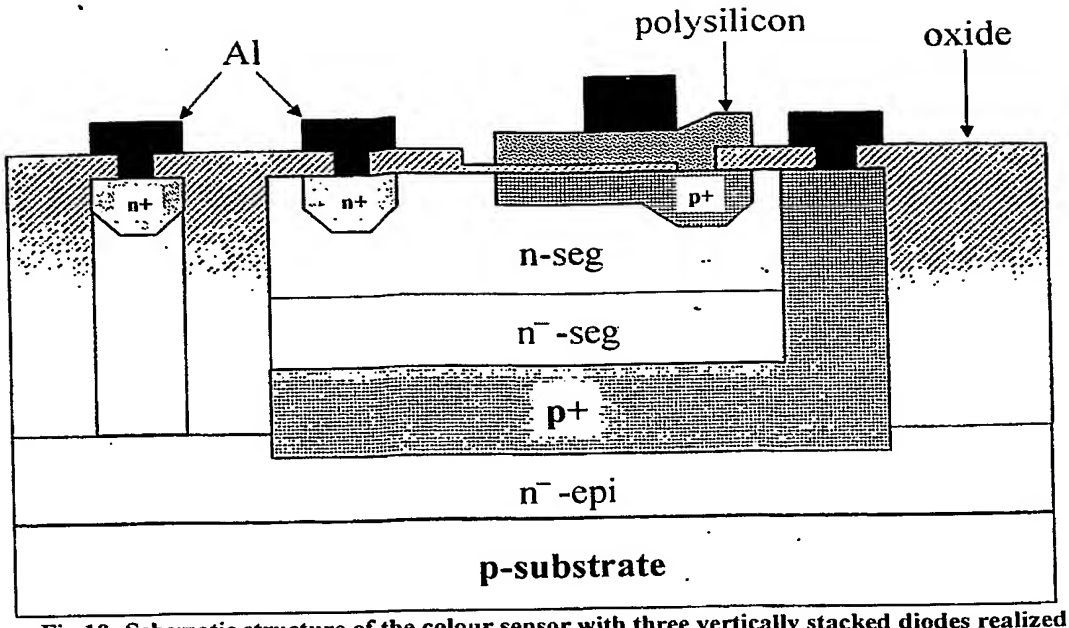


Fig.10: Schematic structure of the colour sensor with three vertically stacked diodes realized using SEG [10].

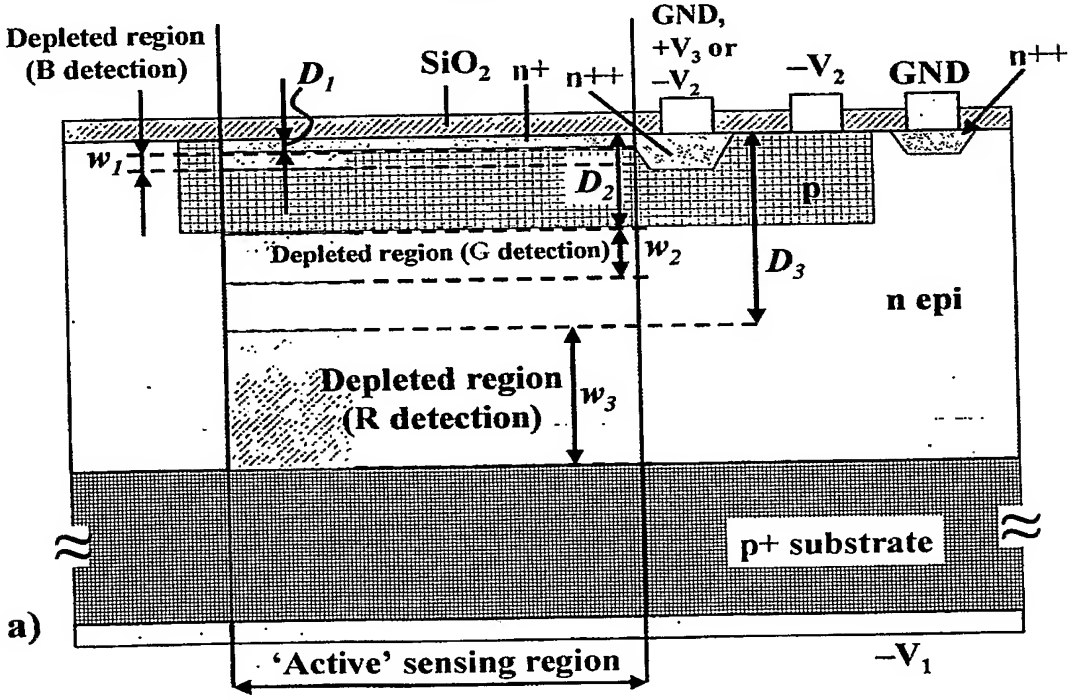


Fig.11: a) Cross-section through the ideal structure of the monolithic three-junction colour sensor, whose concept was initially proposed in EEE-NTU by Assist.Prof. Poenar Daniel and his Ph.D. student, Mr. Chen Jun.

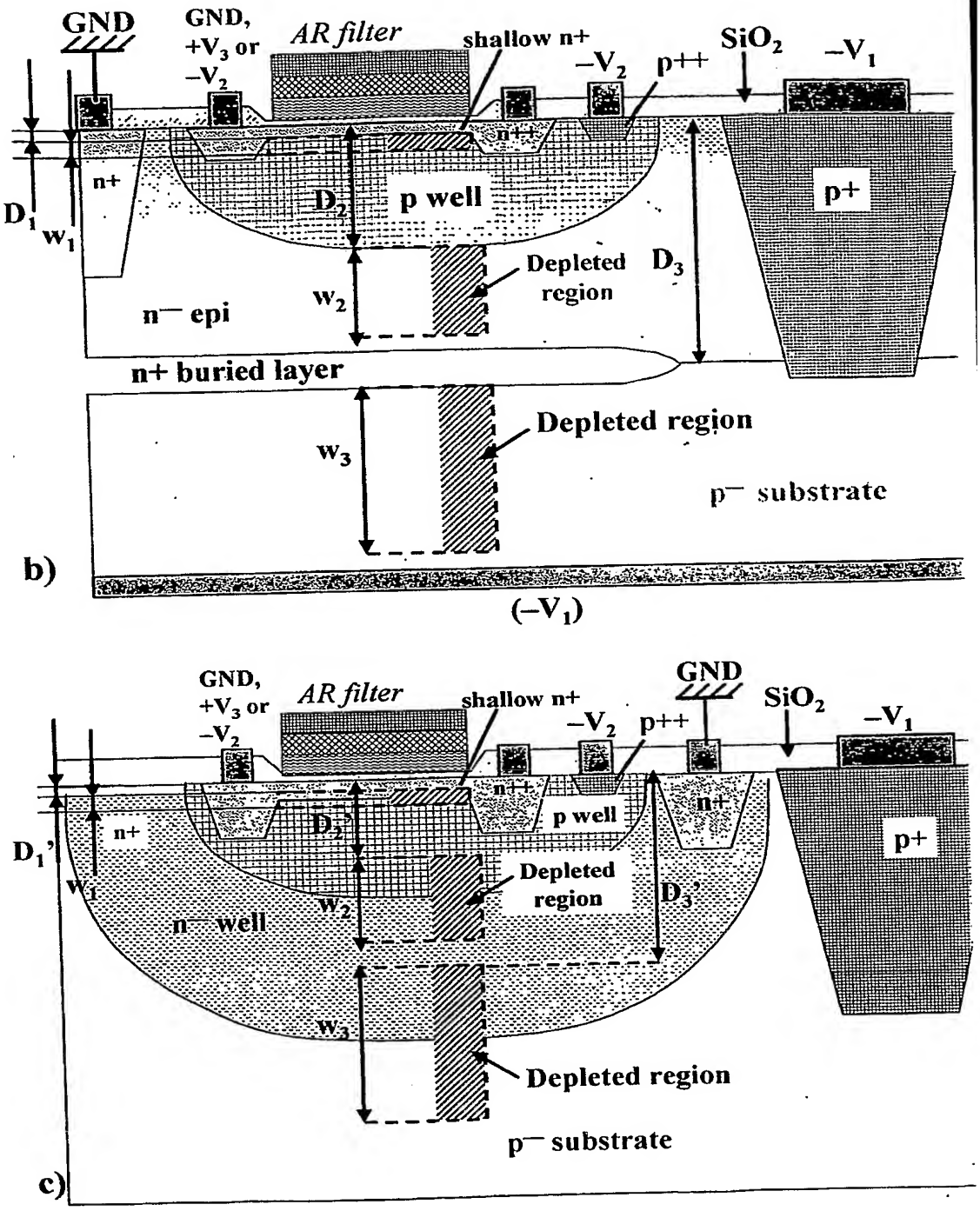


Fig.11 (continued): Cross-sections through the structures of the actual versions that can be practically implemented for the monolithic three-junction colour sensor: b) Abrupt junctions version, and c) Linearly graded junctions version, respectively.

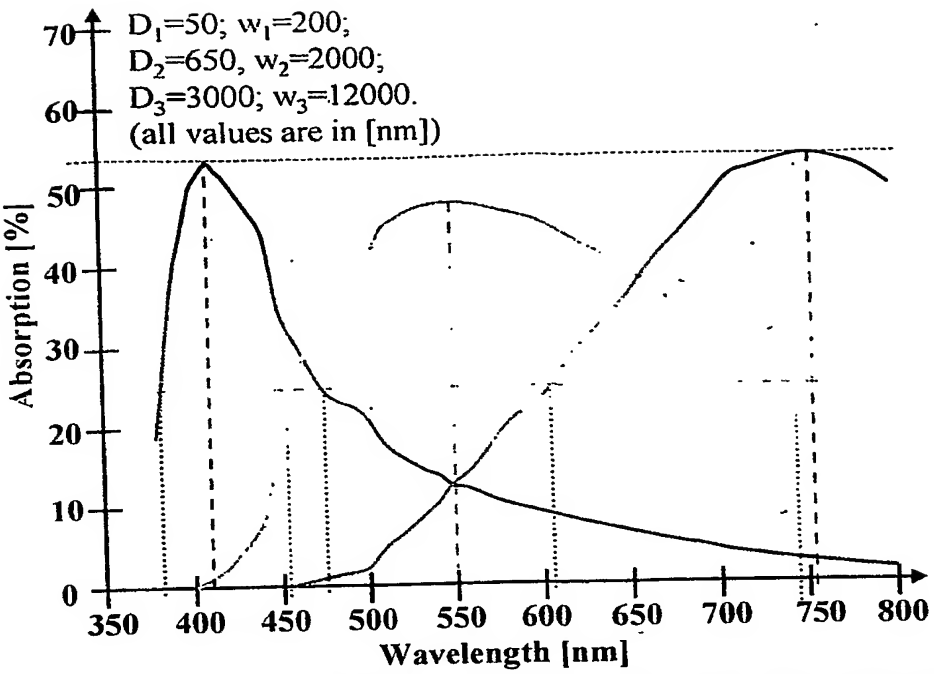


Fig.12: Spectral selectivity curves for the light absorption in each junction's depleted region of the three-junction colour sensor. D and w represent the depth of each junction and the width of its corresponding depleted region, respectively.

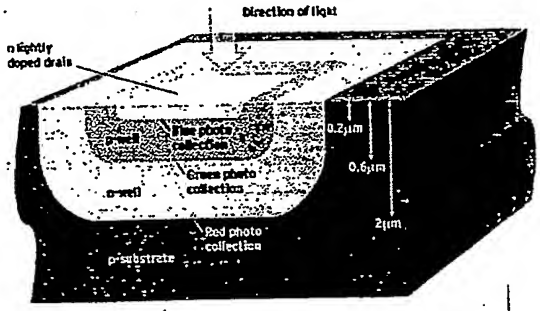
Tricolor Sensors Create a Sharper Image

Stacked three-color pixel is key to Foveon's innovation

IMAGING • Color images shot by a digital camera don't get the full picture. Of the three colors—red, green, and blue—that make up a full-color image, only one is detected by each pixel in the camera's image sensors. The colors from each of the three one-hue pixels have to be combined by mathematical interpolation, which not only adds expense but can inject odd color artifacts quite unrelated to the scene being photographed.

Life may be simpler with the X3 image sensor from Foveon Inc. (Santa Clara, Calif.), in which each pixel is individually sensitive to all three primary colors. Its X3 image sensor (a single pixel is shown right) is said to produce sharper images, enhanced color, and, of course, no unwanted color artifacts. The novel technology "could potentially make a big difference in the [camera] market," says Brian O'Rourke, senior analyst at the Cahners In-Stat group (Scottsdale, Ariz.).

The first application of the X3 chips will be in the new SA9 single-lens reflex camera announced by Sigma



Each pixel (above) in Foveon's new X3 image sensor captures all three primary colors. The sensor is a stack of silicon layers, each doped to absorb different wavelengths of light at different depths. Photodiodes are embedded at the interfaces between layers. In other sensors, each primary color is captured by a separate pixel.

(IEEE Spectrum, May 2002, p.23)

Fig.13: The first page of the article showing the recently patented 3-junction colour sensor for high-resolution digital cameras [14]. Notice the exact identity of both the operational principle and the device structure with that suggested in Fig.10.

spectral characteristic of the ideal device in Fig.11-a, for optimized values of the junction depths D and depleted region widths w, as is also described in Fig.10. One can immediately notice that the device of Fig.11-a, although similar in concept with that shown in Fig.10, is simpler in structure. Moreover, its realization may not require uncommon technologies, like SEG, but can be fabricated using simple diffusion which is easily available in any standard processing environment. Obviously, different spectral selectivities may be developed starting from this initial structure, using different junction depths and/or depletion region widths.

Nevertheless, the ideal concept depicted in Fig.11-a cannot be directly implemented 'as-is' into a practical device. Taking into account other practical considerations besides those related purely to the desired spectral selectivity (e.g. how to realize a good electrical contact with each doped region), resulted in the two practical versions shown in Fig.s 11-b and –c. It can be seen that in each case there are some significant differences from the original theoretical concept.

The "abrupt junctions" version assumes that the junctions can be optimally approximated by using the abrupt models, and therefore the fabrication sequence for this version tries to produce doped regions with the profiles that can most closely match such an assumption. In order to achieve this goal, i.e. profiles as "abrupt" as possible, a buried layer, epitaxy, shallow implantations and short anneals are employed. The ultimate goal is to achieve reasonably "abrupt" junctions located at the depths, and with depleted region of the widths of the same values as indicated in Fig.12. On the other hand, the "linearly graded junctions" version employs diffusion only, and consequently results in smoother doping profiles. This may result in a less demanding processing, but which has a higher thermal budget, and results in extended depths and lateral spreads of the junctions (particularly the deeper ones), thus preventing any severe reduction of the minimal size of such a device. But the most immediate and obvious change imposed by the linearly graded profile of the junctions is the necessity of imposing different junction depths. For the previous "abrupt junction" design, one could safely assume that each value of D_i is exactly the depth of the respective junction, due to the "abrupt junction" hypothesis that implied that in a highly asymmetric junction, almost the entire depleted region extends only in the low doped region. Hence, the immediate equation between D_i and the junction depths on one hand, and between w_i and the width of the depleted regions (extended exclusively in the lower doped regions of each junction) on the other hand, respectively.

However, the things are different for the "linearly graded junctions" version. In this case, the depleted region will extend on both sides of the junction, in approximately equal parts. Consequently, as it can also be seen in Fig.11-c, the junction depths D_i' in this case must be different from the previous values of D_i, and can be calculated as: $D_i' = D_i + w_i/2$

To summarize, Table 1 shows briefly the main values for the various junction parameters of interest for each version of the three-junction colour sensor.

a	Substrate (N_A)	Buried layer (N_D)	*n*-epi	*p*-well	Shall w *n*
Junction depth (or layer width) [μm]	-	1.85	4.5	0.85...0.9	0.06..0.07
Surface conc. (or constant doping for buried layer or substrate) [cm^{-3}]	10^{14}	10^{18}	4.5×10^{14}	$4...5\times10^{15}$	6×10^{16}

b	Substrate (N_A)	Buried layer (N_D)	*n*-well	*p*-well	Shall w *n*
Junction depth [μm]	-	-	6.5	2	0.19..0.2
Surface conc. (or constant doping for buried layer or substrate) [cm^{-3}]	10^{14}	-	$4...5\times10^{15}$	6×10^{15}	6×10^{17}

Table 1: Practical values of the d ped regions parameters f r the two versions of three-juncti n colour sensors: a) The "abrupt junction" design; b) The "linearly graded junctions" version.

The values of x_j obtained for the "abrupt junction" design are different from the desired D_i values due to limitations of real fabrication and other practical problems typical to silicon processing.

Consequently, during the design, simulation and optimization work carried out for these two versions of the three-junction colour sensor, the limitations of such a structure gradually became clearer. Even when simple epitaxy can be used, the triple-junction structure always brings with it three important problems that need to be considered:

a) Finding a solution for contacting all the regions. One easy alternative is to use the substrate as one contact region and use a metal contact on the wafer's backside. This is possible and implementable practically (as shown in Fig.11-a) but it is not the common solution used for ICs and thus can be used only for very large, stand-alone discrete devices.
b) Separating and insulating various pixels from one another. If many identical sensors are used as pixels in a large array, one must effectively insulate each device from one another. This is a most vital aspect that needs to be considered and addressed when using the sensor as a pixel in a large imaging array.
c) Moreover, if all the regions must be contacted only from the top surface, then the large size of the device becomes a significant limitation: the sizes of the diffused areas and their contacts need to be added to those of the insulating structures separating adjacent devices. Moreover, the lateral diffusion spread, especially for the deep diffusions, necessitates large safety margins between the contact regions and the actual device. This results in a smaller active area as compared to the entire chip area (smaller fill factor), and this aspect becomes crucially important when small sensors have to be used as pixels in large size arrays comprising of numerous ($\sim 10^6$) identical elements.

Therefore, a 3-junction colour sensor realized using simple epitaxy and/or diffusion only is more attractive than the SEG-based one, and can be implemented. However, for large imaging arrays employing pixels based on this multijunction approach, then the above listed isolation- and size-related concerns become essential, and, combined with a too complicated technological process, may compel the designer to look for other, simpler and more suitable solutions.

These are the main reasons which determined the search for a new and simpler device which could be efficiently used for colour sensing, even in big arrays constituted of a large number of elements. However, there also was another very important reason which determined not only designing new versions of the 3-junction sensor (as shown in one of the proposed patents) but also searching for an altogether novel colour sensor: the initial simple concept shown in Fig.11-a was patented as a three-well device structure similar to that shown in Fig.11-c, and publicly unveiled in IEEE Spectrum magazine [14], as it can be seen in Fig.13 (see also the subsequent Patent Search, in Section 3.2.2). Although this had a set-back effect on the project by strongly imposing that new versions and implementations should be found and explored, this finding also had a benefic effect. It highlighted that colour sensors are extremely important and that they do make up for an extremely hot topic, at least in what concerns high resolution digital imaging. This only emphasizes once more the stringent need for innovating such novel colour sensing devices and patenting them in an economically short time. At the same time it also clearly explains why we have undertaken the present serious effort for developing and patenting new versions of the three-junction colour sensors, as well as the totally novel JFET-based type of colour sensors, which will be presented in great detail in the next sections.

Finally, it must be highlighted that other materials and principles can be employed to implement colour sensors, too, such as SiC [15], amorphous Si (a-Si:H), or a combination of these two [16, 17]. Amorphous Si in particular seems very suitable for applying the two basic principles of realizing colour sensors previously presented. Thus, a colour sensor realized using *pin* diodes in a-Si:H was reported to detect four basic colour components of the visible spectrum (each of them detected in a separate diode with a different thickness of the *i* region) [18]. The reverse-bias scanning technique was also employed for a colour sensor realized in a-Si:H by employing *pin/pin* vertically stacked junctions with a spectral sensitivity controlled in the entire visible range by the applied bias voltage [19]. However, it is clear that in such approaches employing other materials than monocrystalline silicon, both processing and material limitations strongly impede fabrication compatibility with the standard processing available in EEE-NTU for the realization of on-chip integrated smart sensors. Moreover, the amorphous nature of the material does limit the signal-to-noise ratio (SNR) due to the important leakage currents that appear in such sensors.

2. The JFET-based optical sensors

2.1- The basic JFET

One of the simplest and most well known electronic devices is the Junction Field Effect Transistor (JFET), whose structure and symbol are shown in Fig.14. This device, initially proposed by Shockley in 1952, is in essence a resistor whose conductive cross-section is electrically controlled by the width of the charge region of a reversed biased *pn* junction. The *p*+-doped regions, although in principle can be contacted separately, are connected together and form the gate of the device, whereas the two *n*+ regions form the drain and/or the source. The JFET is a unipolar device employing only majoritary carriers, and it offered a few advantages over the bipolar devices, such as: high input impedance (due to the reverse biased G-S junction), faster switching time and reduced temperature dependence (as it does not rely on minority carriers in its functioning), very low noise, and no offset leakage current (i.e. I_{DS}=0 when V_{DS}=0). However, unlike the bipolar devices it does not have a current gain and the a.c. amplification it offers is smaller. Nevertheless, the JFET is a very useful device, especially where high input impedance and/or low noise are required, which makes it a very good alternative for the very first transistors (inverting and non-inverting inputs as gates of two JFET transistors) in the input differential stages of op-amp ICs, as well as in RF low noise (pre)amplifiers, or in microphone preamplifiers.

However, in the last decades its usage was reduced mainly due to the advent and extreme spread of the MOSFET, in which the junction gate was replaced by a Metal-Oxide-Semiconductor (MOS)-based one. Fig.15 presents the structure of such a transistor, as well as its most important characteristics. (Note: in both Fig.14 and Fig.15 only *n*-type channel devices are presented, but the complementary *p*-type channel can also be realized). The output characteristics of the JFET are similar to those of the MOSFET, presenting two regions: linear (or 'triode'-like) and saturation. The equations describing the dependence $I_{DS}=f(V_{DS})$ for the output characteristics of a JFET are:

$$I_{DS}=\begin{cases} G_0\cdot\left(1-\sqrt{\dfrac{V_{GS}}{V_T}}\right), & for \quad V_{DS}<V_{DS,Sat} \\ I_{DSS}\left(1-\dfrac{V_{GS}}{V_T}\right)^2, & for \quad V_{DS}>V_{DS,Sat} \end{cases} \qquad (7)$$

where $V_{DS,\,Sat}$= the drain-to-source voltage starting from which the device enters the saturation region (i.e. at which the channel is pinched-off in a single point right at the drain location) = $V_{GS}-V_T$, and V_T = the cut-off voltage (i.e. the gate voltage for which the channel is completely closed by the depleted regions) given by the relation

$$V_T=-\frac{a^2qN_D}{2\varepsilon}+\Phi_{B0} \qquad (8)$$

in which ***a*= half of the total (unbiased) *n*-channel height**, N_D= the donor doping concentration of the channel and Φ_{B0}= the gate-source junction's built-in potential.

In eqn. (7) G_0 is the conductance of the *n*-channel of width W and length L at V_{GS}=0:

$$G_0=q\mu_nN_D\frac{2aW}{L} \qquad (9),$$

For very small V_{DS} voltage values the transistor can be used as a voltage controlled resistor, and in this case the dynamic resistance exhibited by the device can be approximated as

$$r_d=\frac{r_0}{1-K\cdot V_{GS}} \qquad (10)$$

where $r_0=1/G_0$ and K= a constant typical to each device.

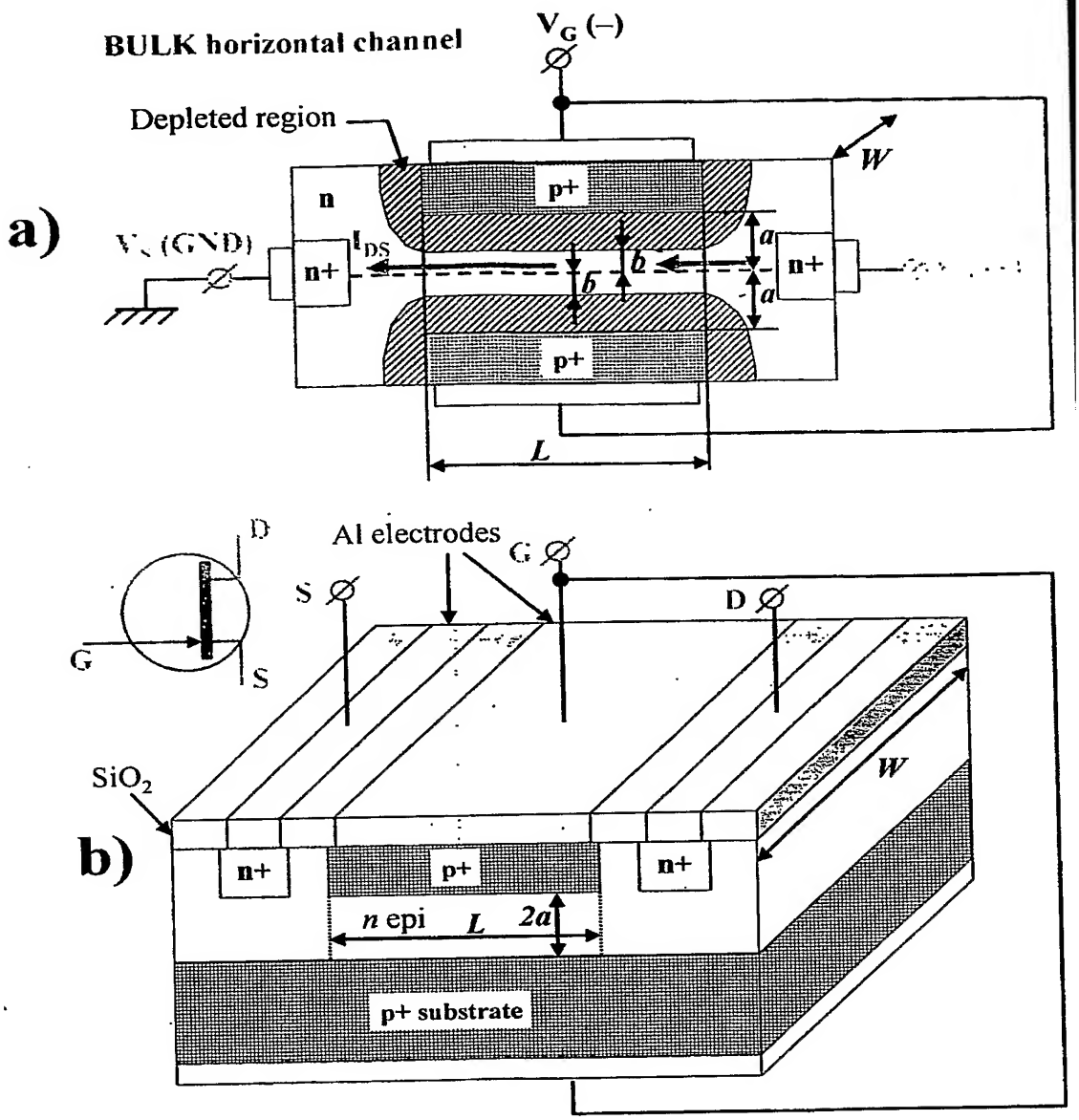


Fig.14: a) The simplified structure of an *n*-channel JFET, highlighting its basic operating principle; b) The structure of a real device and its symbol.

2.2- The JFET-based optical sensors

Just like the normal diode, the bipolar transistor and the MOS structure, the JFET can also be transformed into an optical sensor. For the other devices the resulting structures for optical sensing purposes are the photodiode, the optotransistor and the CCD, so the existence of JFET-based optical sensors should not be a surprise. However, as these JFET-based optical sensors are less common and much less known, we shall briefly summarize here the results of our literature review in order to present to the reader this type of optical sensors.

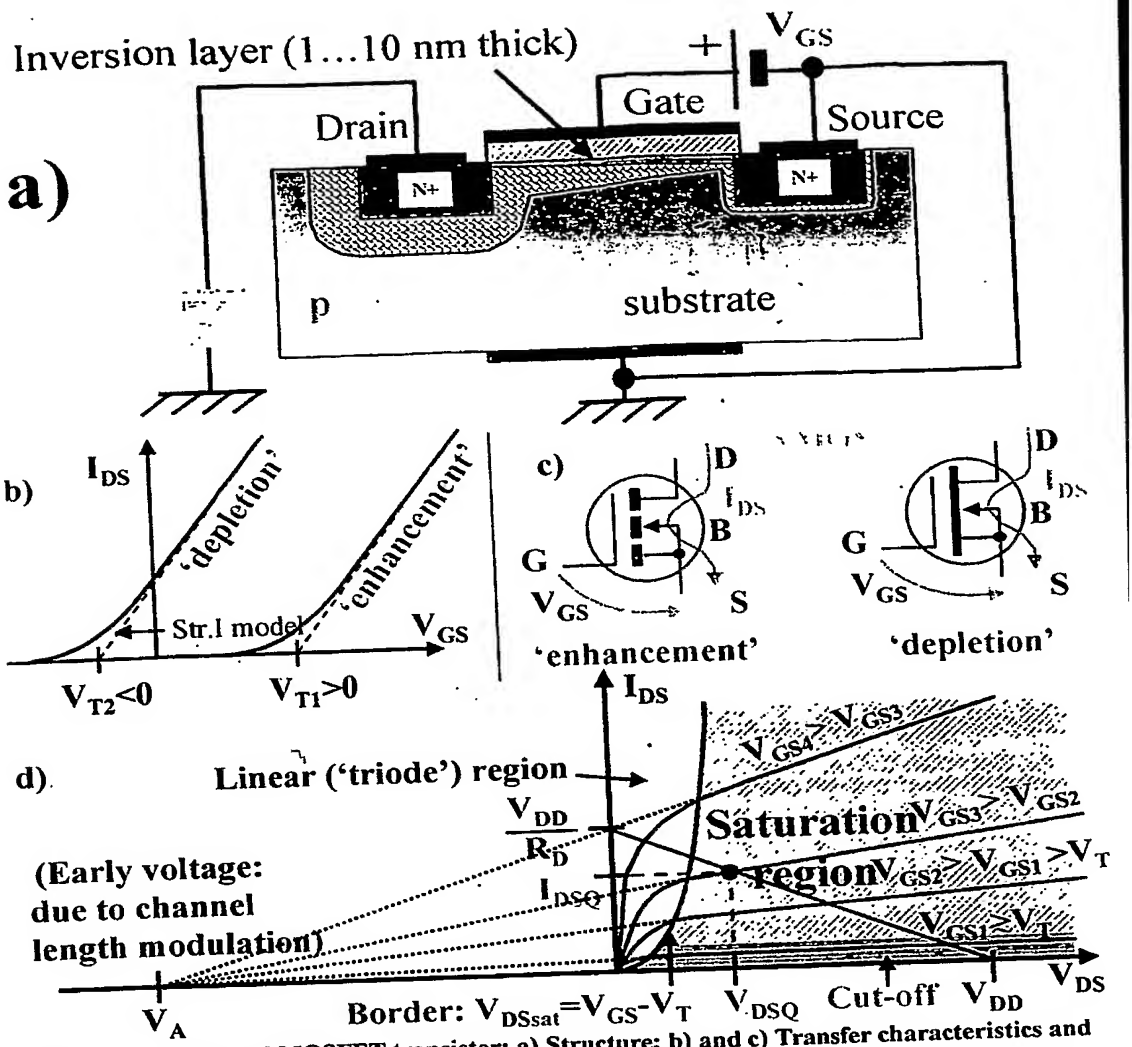


Fig.15: The *n*-channel MOSFET transistor: a) Structure; b) and c) Transfer characteristics and symbols of the enhancement- and depletion-type of devices, respectively; d) Output characteristics of an enhancement NMOS transistor.

2.2.1- Literature review

2.2.1.1- The PhotoJFET

S.G. Bandy and J.G. Linvill developed one of the first photo-JFET mentioned in literature, shown in Fig.16 [20]. This field effect photodetecting structure was conceived as a stand-alone device capable of producing an output voltage on the order of volts that is linearly related to incident illumination intensity.

The top and bottom gate are connected at the same potential V_G since they connect in order to completely enclose the channel. If the top gate has a thickness less than the diffusion length L_n of its minority carriers, then the junction collects all carriers generated by the incident light in the top gate so that the top gate and channel form an effective photodiode.

The design for such an optimum field-effect photodetector has to maximize its channel impedance (responsivity), subject to constraints of surface area and deviation from linearity over a

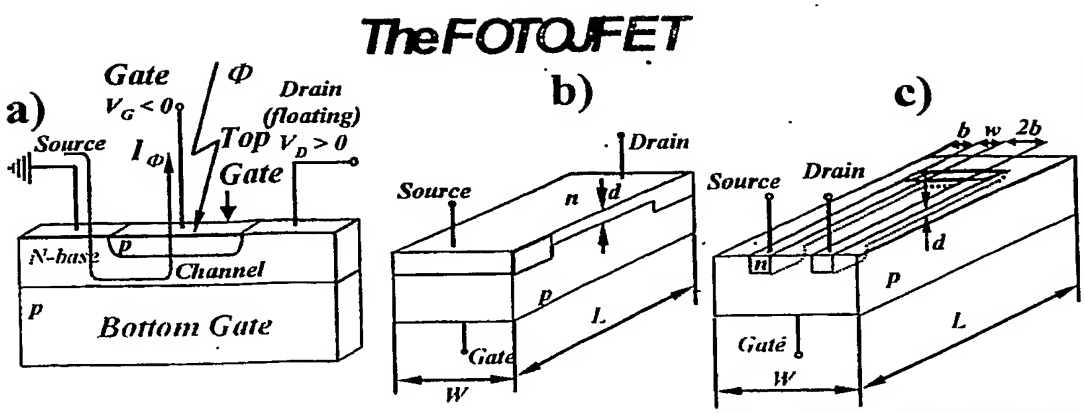


Fig.16: The JFET photodetector [20]: a) Schematic basic structure; b) Conventional geometry with an aspect ratio *W/L*; c) The "maze" geometry for RBW comparisons- aspect ratio= *W/2L*.

specified range in drain signal. The described photoJFET corresponds to the impractical classical scheme for photodetection using a photodiode in series with resistor having a high resistance, both components being integrated in a single solid-state device. The impedance of this device is voltage-controlled over a range extending, for all practical purposes, to infinity. Both of these features substantially reduce the surface area from what would be needed for an equivalent photodiode-resistance series combination. The basic motivation for conceiving this JFET photodetector was to provide a single device that could produce output voltages comparable to devices operating in charge storage mode for the same illumination levels, but yet to avoid the switching problems of inherent in the latter type of realizations, especially at low light levels. In this charge-storage mode the gate–channel junction is charged with a gate pulse and then left floating, so that any illumination discharges the junction, with the channel width and hence the current drain being proportional to the total illumination integrated over a period of time. The simplicity of fabrication, the possibility of achieving larger responsivity-bandwidth (RBW) products by using a "maze"-type of layout for both the S/D & G, as well as real time operation are assets of the JFET photodetector that make it more amenable to certain applications than other types of photodetectors.

The "maze" structure allows a longer channel length *l* and smaller channel width *w* for the same total device area *WL*, thereby increasing both R_0 and the responsivity, the authors claiming a resulting responsivity proportional to the square of device area.

The above mentioned paper [20] also highlights the advantages offered by the JFET as an optical photodetector:

- Can work in three operational modes:
  - photoconductive (S&G shorted);
  - photovoltaic, i.e. as photodiode (S&D shorted);
  - phototransistor (with gate bias, as a usual JFET, measure, e.g., variations in I_G);
- Operating the photoJFET beyond the gate cutoff voltage V_{GC} one can obtain a photoresponse independent of almost all device parameters, including surface area => very small area devices can be practically obtained without (theoretically) any significant loss in sensitivity. At the same time, the channel will essentially present an infinite impedance to the photocurrent I_F.

2.2.1.2- The SIT and FCT: basic structures

Another type of JFET-based structure is the Static Induction Transistor (SIT) proposed by Jun-ichi Nishizawa [21]. It is actually a **vertical** JFET wherein carriers are injected from source to the drain across a potential barrier induced in a current channel and wherein the height of the potential barrier can be varied in response to a gate bias voltage applied to a gate and to a drain bias voltage applied to the drain to thereby control the magnitude of a drain current of the transistor. The SIT has the advantage that its current-voltage characteristic curve is nearly linear over a very wide range of drain currents, including the low drain current region. A very similar structure, called Field-Controlled

Thyristor (FCT), was introduced by J. Baliga [22], which is almost identical to the SIT, the only difference being that, unlike the SIT, which is a unipolar device, the FCT is a bipolar one.

The simplified structures of both these types of devices, shown in Fig.17, were –and still are- proposed and used for power applications. Its main advantage over classical electronic switches for high power applications, e.g. thyristor and even Bipolar Junction Transistor (BJT), is the capability of being switched off, and in a relatively short time. In the case of the SIT this switch-off time is relatively short because the entire device is unipolar and the gate can efficiently strangle off and extinguish the total drain current. In the case of the FCT the switch-off time is longer as the development of the depletion regions around the gate regions can begin only after evacuating the stored minority carriers. Even so, if the gate circuitry is specially designed to be able to evacuate such a large amount of charge in a short time, then the field-effect of cutting-off the current by development of depleted regions by the gate regions will also appear. Therefore, at the time of their apparition, the overall switch-off time of SITs/FCTs were more advantageous than those exhibited by BJTs or GTOs (Gate-Turn-off Tyristors) existing at that time.

However, a main disadvantage of this type of devices, in contrast to the classical transistor and thyristor, is that they are normally OFF, an inherent feature due to the JFET-based structure. However, with the gates now vertically placed, reducing the layout feature sizes to submicron levels in conjunction with using extremely low doped substrates and a mosaic-type of layout with many small but parallel connected drain regions, allowed the creation of normally OFF devices, in which the built-in depletion region of the gates extends sufficiently from one gate to its next neighbouring region so as to block the flow of the current even without any applied gate bias. Of course, such a solution requires expensive high-end photolithographic processing, which can lead to high production costs that are justified only for large-scale mass production. Moreover, having a vertical diffusion for the gate, means that the doping (along the depth of the device) of this gate region is nonuniform, and this also may have consequences for its power applications, namely its capability of switching the device from fully ON to OFF. In order to eliminate this auxiliary problem, special epitaxial growth recipes were developed: the gate regions were first etched in the *n* epi and then refilled with strongly doped

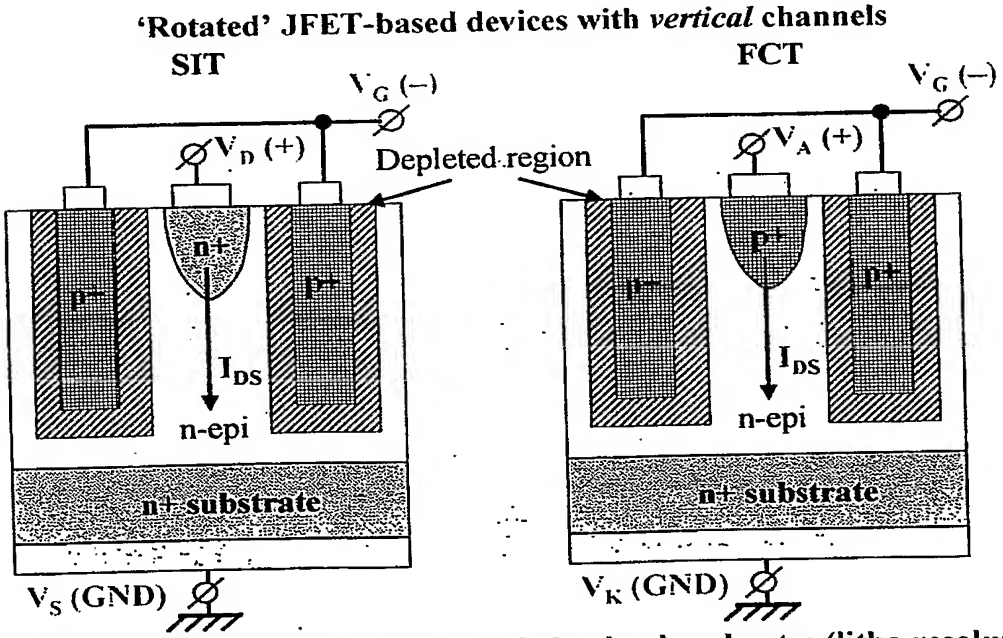


Fig.17: Schematic representation of vertical JFET-based devices: the SIT and the FCT, respectively.

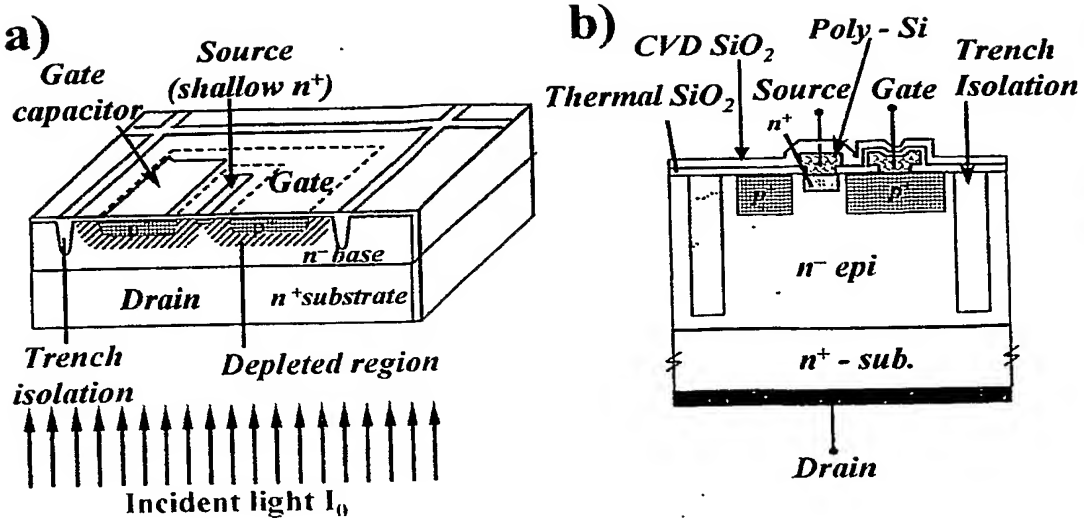


Fig.18: Schematic diagram of the SIT-based image sensing cell: a) 3D-like simplified layout view; b) Close-up cross-section of the device [23].

epitaxially-grown p^+ Si. Obviously, this solution also required special equipment and dedicated know-how.

However, in this case we are far more interested in the optical related applications of such devices as sensors. Before going into depth in such a direction, let's continue the summary of other JFET-related optical devices existing in literature.

2.2.1.3- The SIT-based image sensor

A new type of SIT-based optical sensor was proposed by the same Jun-ichi Nishizawa and his coworkers [23]. By selecting appropriately the impurity concentrations and thicknesses of the various device regions, the authors easily attained and exploited the above-mentioned properties and advantages offered by the SIT structure. It is worth noting that the device is a backside-illuminated one, and its full structure is presented in Fig.18.

Nishizawa's work indicates how one can optimize some characteristics such as the series resistance of device from the source to the intrinsic gate (the region in which the drain current is substantially controlled). In addition, for a low impurity concentration of the channel region and a small width of the channel region the depletion layer extends from the gate so as to form an intrinsic gate of potential barrier type, and to pinch off the channel region. Also, the gate length is designed to be short in order to provide a very small series resistance. The height of produced in the intrinsic gate region can be controlled by varying either the gate (G) or the drain (D) potential. For this reason, the SIT is able to exhibit a non-saturating type of I-V characteristic. Moreover, its gate capacitance can be reduced drastically by using a very small gate length, which makes it highly suitable for high-speed and low power dissipation operation.

A high sensitivity semiconductor photoelectric converter can be obtained by electrically isolating the gate region of the SIT which exhibits the non-saturating I-V characteristic, as this enables the enlargement of the output current simply by increasing the drain voltage. Optically generated minority carriers are stored in the insulated gate region to control the potential thereof. The fact that in this case the device is provided with a gate capacitor (i.e. basically combining the SIT with an MOS structure) is very effective in enhancing the dynamic range of the photoelectric conversion. Consequently, an integrated image pick-up device can be constituted by further combining these two elements with read-out circuitry.

However, if the amount of light irradiated on the device is not abundant, the stored electric charge will be small. Therefore, it is typically not possible to obtain a large signal with such devices if the light is weak. Furthermore, leakage of the stored electric charge often occurs when it is being transferred. The detection of light, however, is carried out by utilizing the *pn* junction at the source region as a photodiode. Therefore, this image pick-up device has the same problems similar to those exhibited by existing charge transfer devices, namely limited light sensitivity.

Integrating a multiplicity of the static induction type photoelectric converter elements can materialize a high-speed and high sensitivity image pick-up device. A switching transistor may be merged in the gate region of each photoelectric converter element to enhance the operation speed of the image pick-up device.

The authors realized the new SIT-image sensor in an IC configuration suitable for standard TV format and they confirmed experimentally its operation and operational characteristics. The authors claim that the features and advantages offered by this SIT-based imaging sensor are:

- Larger sensitive area: the narrow isolation region widens the aperture area with no charge loss;
- Wide dynamic range of wavelengths and intensities: the authors claim a relatively high generation rate even for violet-blue light (short wavelengths) because of the high efficiency of charge collection in the n^- epitaxial area which covers 45% of the pixel);
- Low-noise (very low power for a stable switch operation, low leakage current);
- Non/semi-destructive readout;
- High-speed performance (3.5 ns @ 200 μW bias and a gate size of 10 μm × 10 μm);Very simple structure and small pixel size!

2.2.2- Patent search

The first stage in the patent search was using the website of "United States Patent and Trademark Office": http://www.uspto.gov. The first search in the Issued Patents (PatFT) was carried out using the keywords "Junction Field Transistor "**and** "color sensor" but no patents were found. The second search used "Junction Field Transistor " **OR** "color sensor", which resulted in 1085 patents, most of them refering to composite materials or semiconductor devices using polymer filters. The following sections will highlight only the few patents which we selected to be truly relevant for our topic: colour sensing in a silicon-based semiconductor device employing a JFET-based (or related, e.g. SIT- or FCT-based) structure, and operated correspondingly.

2.2.2.1- Vertically-stacked multijunction sensors

We shall first start the review of the results of our patent search by examining those documents which are the least related to our devices, but still bear some resemblance, either in structure and/or in functionality, with the sensing devices that we shall propose in the next section.

One such patent introduces a semiconductor-based polychromatic image sensor for converting an optical signal into an electrical signal [24]. The sensor is provided with at least two *p-n* junctions of which the depth from a light incident plane varies continuously, and a plurality of such sensors may be arranged into an array. The operation of this polychromatic image sensor is clearly based on the dependence on wavelength of the light absorption in silicon, as it was previously explained in section 1.2.1 (see again Fig.s 3 and 4). Its configuration is shown in Fig.19: the first *p-n* junction 8 can be reached by light of both and long wavelengths, while the second *p-n* junction 9 cannot generally be reached by short wavelengths, which have been already absorbed. Accordingly, information including short wavelength light can be obtained from the first photodiode 10, while information excluding short wavelength light can be obtained from the second photodiode 11. However, as it is apparent from Fig.19, a major feature of this device, which makes it very different from all the other analyzed devices, is that the continuously varying depth of the device is ensured by fabricating a sloped profile of the entire device, which is not the case with any of our proposed devices.

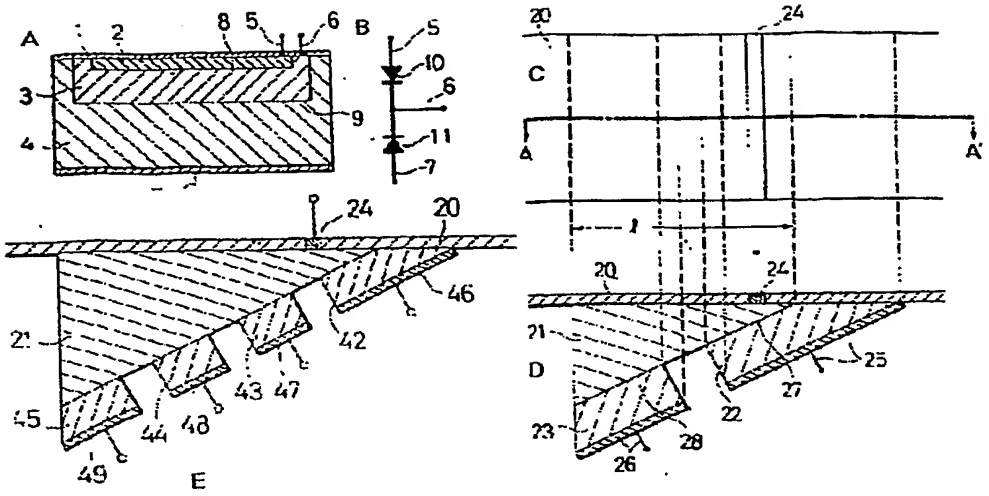


Fig.19: Polychromatic image sensor [24]: A) Cross-sectional view of the device; B) Equivalent circuit diagram of A; C) Layout plan (top view), and D) Cross-sectional view of proposed polychromatic image sensor.

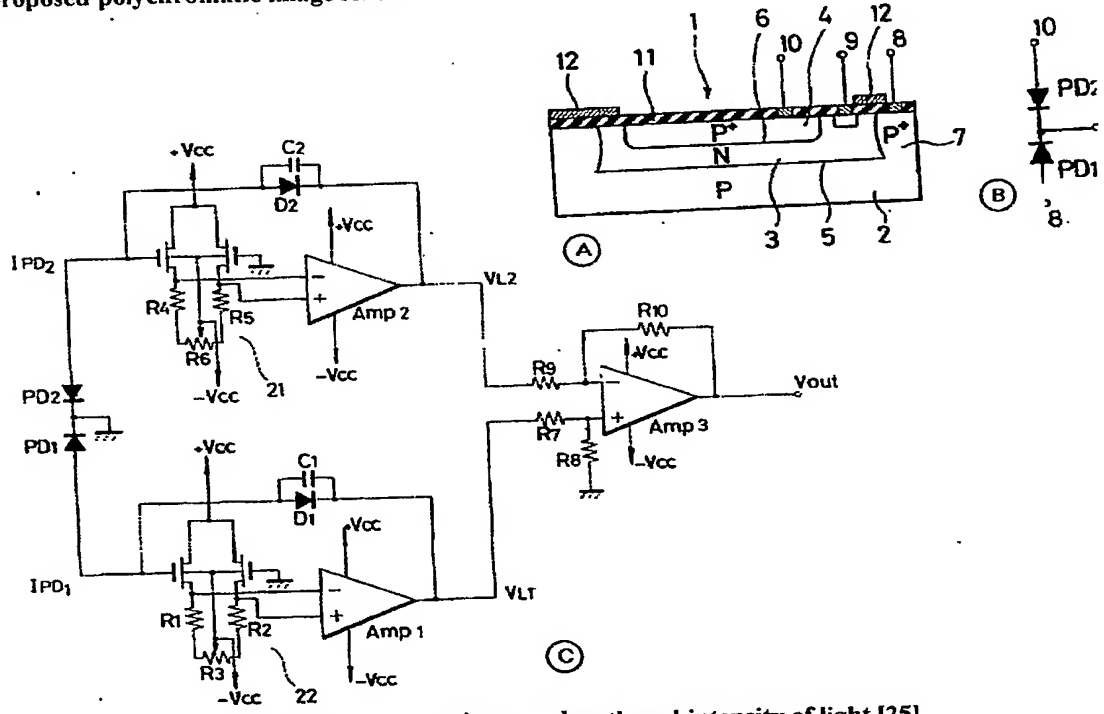


Fig.20: Apparatus for sensing wavelength and intensity of light [25].

Another patented device for colour discrimination, is a solid state wavelength detection system responding to output signals derived from a photoelectric semiconductor device [25]. This photoelectric semiconductor device comprises at least two *p-n* junctions formed at different depth from the surface of the semiconductor substrate. The deeper and shallower *p-n* junctions develop output signals related to the longer and shorter wavelength components of the light impinging thereon,

respectively. These two output signals are then logarithmically compressed and compared with each other. The difference of the logarithmically compressed output signals represents the wavelength information of the impinging light.

The principal objective of this invention is to provide a wavelength detection system implemented with a photoelectric semiconductor device, namely a solid state colour sensor based on a dual junction photoelectric semiconductor device. Drawing 4A in Fig.20 is a cross-section of the patented photosensor, while drawing 4B is a diagram of its equivalent circuit. Finally, drawing 4B is a circuit diagram of an embodiment of a detection system for this invention.

The device operation is as follows: the incident light beam is applied to a photoelectric semiconductor device 51 including a first photodiode PD_1 (6 in Fig.20-A) and a second photodiode PD_2 (5 in Fig.20-A). The output signals of PD_1 and PD_2 are applied to operational amplifiers 53 and 52, respectively. Logarithmic compression diodes D1 and D2 are connected to the operational amplifiers Amp1 and Amp2, as shown in drawing C of Fig.20. The output signals VL1 and VL2 of these operational amplifiers are further applied to a subtraction circuit (with AMP3) and then to an adder circuit (not shown in Fig.20).

A more recent invention relates to optical detection and describes a photodetector with "buried junctions and its method of manufacture" [26]. The invention intends to cover a broader range of applicability, with claims regarding an optical sensor applicable for color imaging, artificial vision, color measurement and spectral measurement systems. The photodetector is based on two successive *p-n* junctions (11 and 12 in Fig.21-a; 111 and 112 in Fig.21-b), buried at increasing depths, assembled in pairs in opposition and thus defining at least three layers 21, 22 and 23, as illustrated in Fig.21-a, or 121, 122 and 123 in Fig.21-b, respectively [26]. One of the layers is adjacent to a photosensitive portion of the surface of the photodetector. A reverse bias is applied to the junctions, and the values of at least two internal currents passing through such junctions is detected. These internal currents I_1, $I_{1,2}$, I_2, and I'_2, $I'_{1,2}$, $I'_{2,3}$, and I'_3, respectively, are generated by received light, with each of the junctions (11, 12, 111-113) being responsible for photogenerrating currents corresponding to a particular wavelength of the incident light 5 falling unto the photosensitive part (34, 131) . Consequently, the spectral responses of these internal currents will exhibit a peak centred at the peak wavelengths that are absorbed at the depth of that specific junction. The structure may also comprise more than two or three junctions whilst at the same time being produced by conventional integrated circuit technology. The spectral information is obtained by placing the junctions at certain depths, thus providing a desired spectral responsivity, with the internal currents photogenerated in the junctions' depleted regions having maxima at certain peak wavelengths according to the exact junction depths. Consequently, the device patented in this invention is a color photodetector, i.e. a photodetector providing information on both the intensity of incident light and its spectral composition at the same time.

The difference between the structures shown in Fig.s 21-a and 21-b, is that the first includes two *pn* junctions, whereas the latter one has three. Another difference is that structure 10 in Fig. 21-a is partially covered on its surface 30 by an opaque metal layer 35. In this way, only a photosensitive part 34 of the first part 31 is exposed to the light, which prevents parasitic photocurrent contributions. Any of the two versions of the photodetector is preferably produced by CMOS technology, although it is equally possible to produce the structure through BiCMOS or bipolar technology. It is advantageous that the two peak wavelengths should be respectively situated in the wavelength ranges associated with the colors blue and red.

Another difference between the structures is that the structure 10 in figure 21a is partially covered on its surface 30 by an opaque metal layer 35. In this way, only a photosensitive part 34 of the first part 31 is exposed to the light, which prevents parasitic photocurrent contributions.

The chip containing the sensors is produced by conventional CMOS technology in an *n*-type well (23 and 123 in Fig.21). This chip includes an array of 3x3 photodetecting cells and on-chip circuitry. Each of the cell has the structure 10, its surface 30 measuring 200x200 μm^2 and having a central exposure window corresponding to the photosensitive part 34 which covers 180x180 μm^2. The on-chip circuitry includes the external circuit 40 (nu e!) and the measuring device 50.

Just like any colour sensor, this one can find various applications, as we have also highlighted previously in Section 1.1. The authors of this patent specify particularly color imagining, e.g. for video cameras producing color images, as well as artificial vision, notably for detection of colors in artificial

retinas. Other possible applications are concerned with colorimetric measurements (for systems such as scanners or devices for matching colors in color printing) and spectral measurement. This latter application relates to the measurement of absorption, emission or reflection spectrum of a solution, a solid or a colored gas or of a smoke, as well as the measurement of the spectral composition of light which is determinant for the measurement of properties of a physical, chemical or biological phenomenon. Consequently, as it was already underlined in Section 1.1, such colorimetric measurements are useful in chemistry (measurement of absorbance, pH measurement of a substance, or indirect measurement through injection of a coloring agent), in biology, biochemistry and medicine, and in environmental applications (gas measurement, pollution detection, measurement of concentration of elements in a solution). This also covers spectro-colorimetry consisting of determining a color spectrum by spectral dispersion.

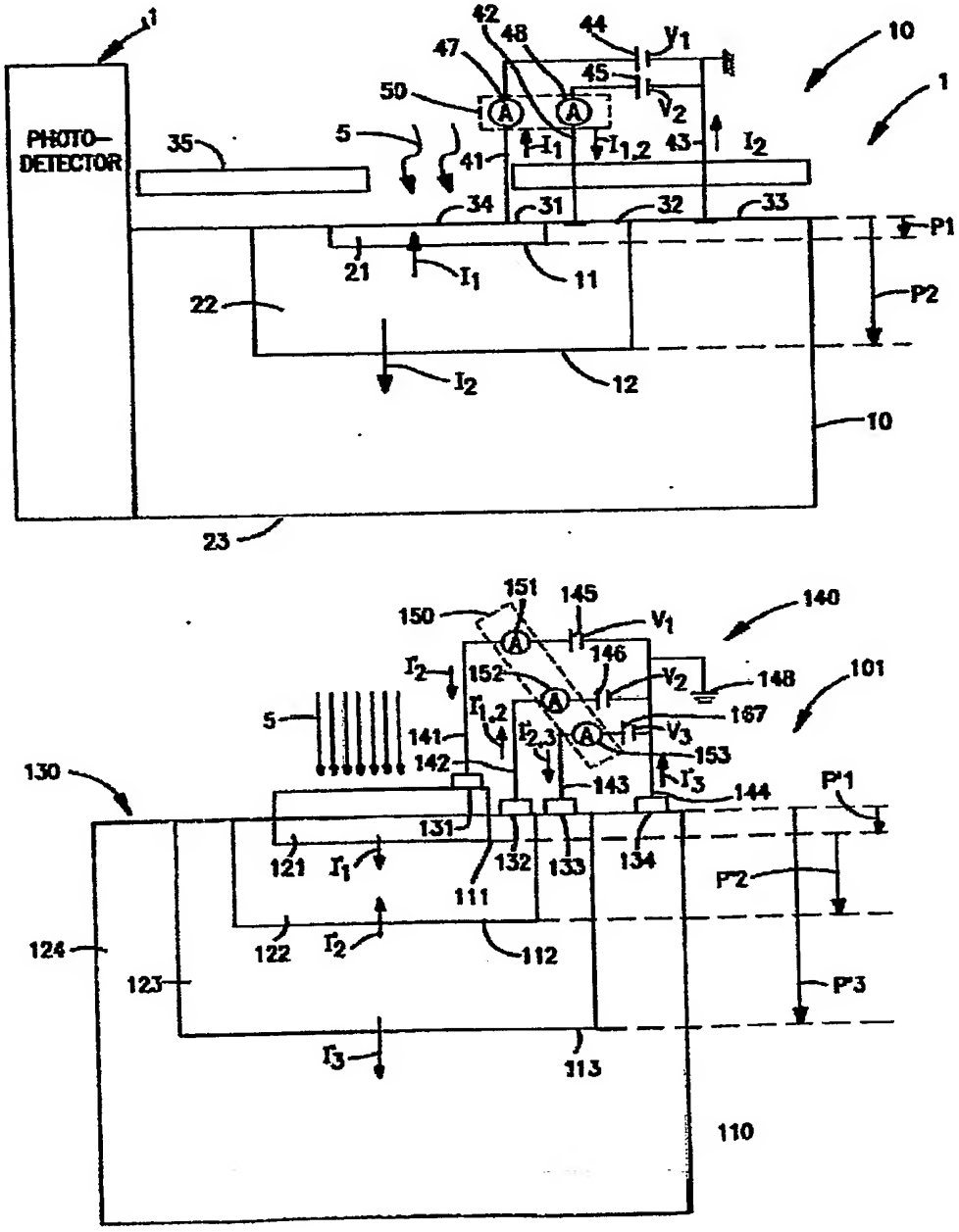


Fig.21: Two versions for the proposed photodetector structure based on buried junctions, with two (top) and three junctions (bottom), respectively [26].

Finally, our patent search for multijunction structures could not be complete without the device formerly presented in Section 1.2.3 (Fig.12). The device consists of the vertically-stacked triple-junction structure already introduced in Fig.11, as it can be seen in Fig.22 [27]. The same differential light absorption along the depth of Si is used, and the only difference from our initial idea is that the authors use different names: "active pixel" and "triple-well", the latter being necessarily mentioned in order to allow the usage of CMOS-related fabrication processes based on the usage of such 'wells', as is openly specified in the patent text. The imaging-related applications are also very clearly targeted, specifically highlighting the lack of color aliasing due to direct measurement of all the three fundamental colors by the same pixel, not by separate pixels placed in different spatial locations as was the case with previous realizations.

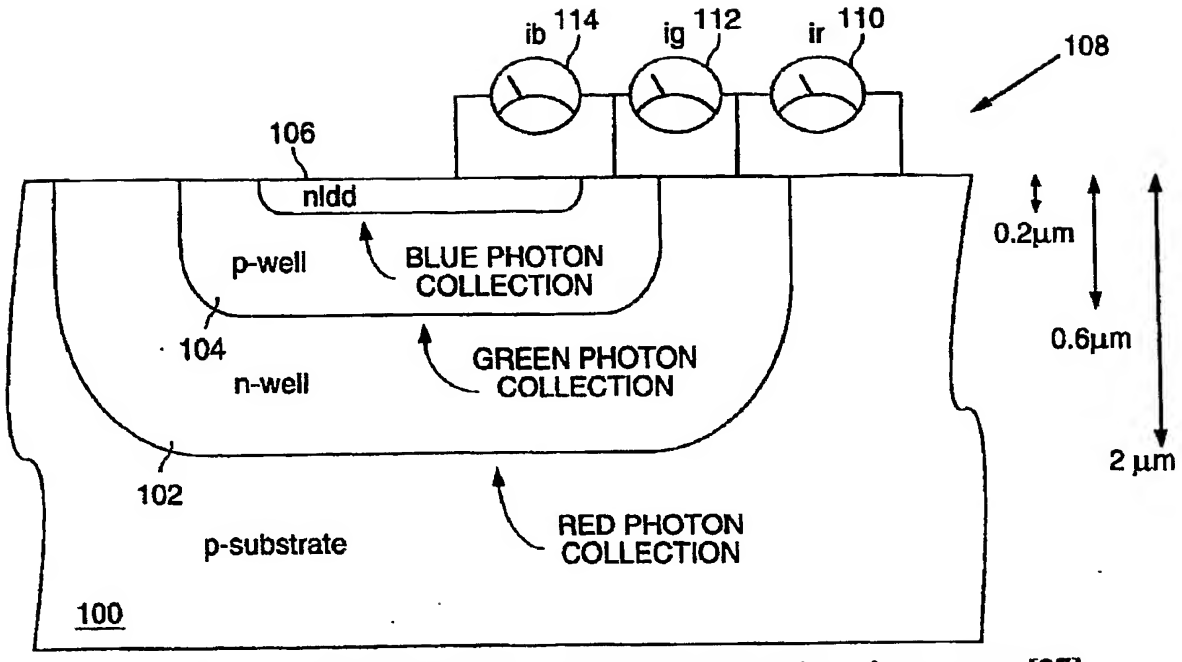


Fig.22: The triple-well active pixel cell for colour imaging arrays [27].

In conclusion, all the multijunction devices presented in this section do indeed claim to offer outputs related directly to the wavelength (i.e. the colour) of incident light (not only to its intensity), and they also have a JFET-type of structure. However, the operation of ALL these device is NOT based on the FET structure, i.e. there is no current flowing **within** the *n* region, **along it** (which should thus have **two** contact regions at its ends, not just a single one), current which may be modulated by the photogenerated carriers (photoconductivity modulation is mentioned in a few patents but NOT related at all to colour sensing). Indeed, all these devices have the same basic structure, which can be interpreted as a JFET-type, but which is operated as a simple photodiode-based complex: the equivalent circuit includes only diodes and there are no Source & Drain contacts for the middle region. Consequently, this structure is essentially a bipolar, not an FET, device. Therefore, other patents were searched for, that could be more closely related to our topic, JFET-based colour sensors.

2.2.2.2- JFET-based sensors

K. Lehovec is the first inventor referring to JFETs and optical JFET sensors [28]. His invention relates to transistor combinations by which signals can be amplified, more particularly to render unipolar FETs either less susceptible to breakdown or, alternatively, susceptible to much higher current gain or improved reliability of operation when used with signal voltages of substantial amplitudes. However, the invention does have a part relating to sensors, and in this respect from his patent we are interested only in drawing F of Fig.23 which shows a form of unipolar transistor useful as a photosensitive device in which the bulk of crystal 91 has one type of conductivity, e.g. *n*-type. When this body is exposed to light, current flows between electrode 93 (in the circular depression) and the bulk crystal 91. This current flow reduces the bias imposed by the battery 95 through resistor 96 (together making a high impedance bias source). Thus the space charge in the semiconductor region adjacent to the depression is reduced, allowing a greater current flow in the channel between electrodes 97 & 98. The voltage source 95 biases the electrode 97 in the current-blocking direction. With the impedance 96 relatively low as compared to the blocking impedance of the un-illuminated junction, the potential of the source is essentially impressed across this junction 94 (between electrode 93 and the bulk of the semiconductor 91). When light irradiation takes place, the impedance of this junction is sharply diminished so that the potential across it is greatly lowered and this cause a corresponding amplified change in the current passing between the output electrodes.

As it is immediately obvious, there are large differences between this sensors and our application. First, and most importantly, although the photoconductivity modulation is mentioned, there is no specific connection related to colour sensing: the device in the patent is only a simple optical sensor which may sense light and probably various light intensity levels, but it is not specifi-

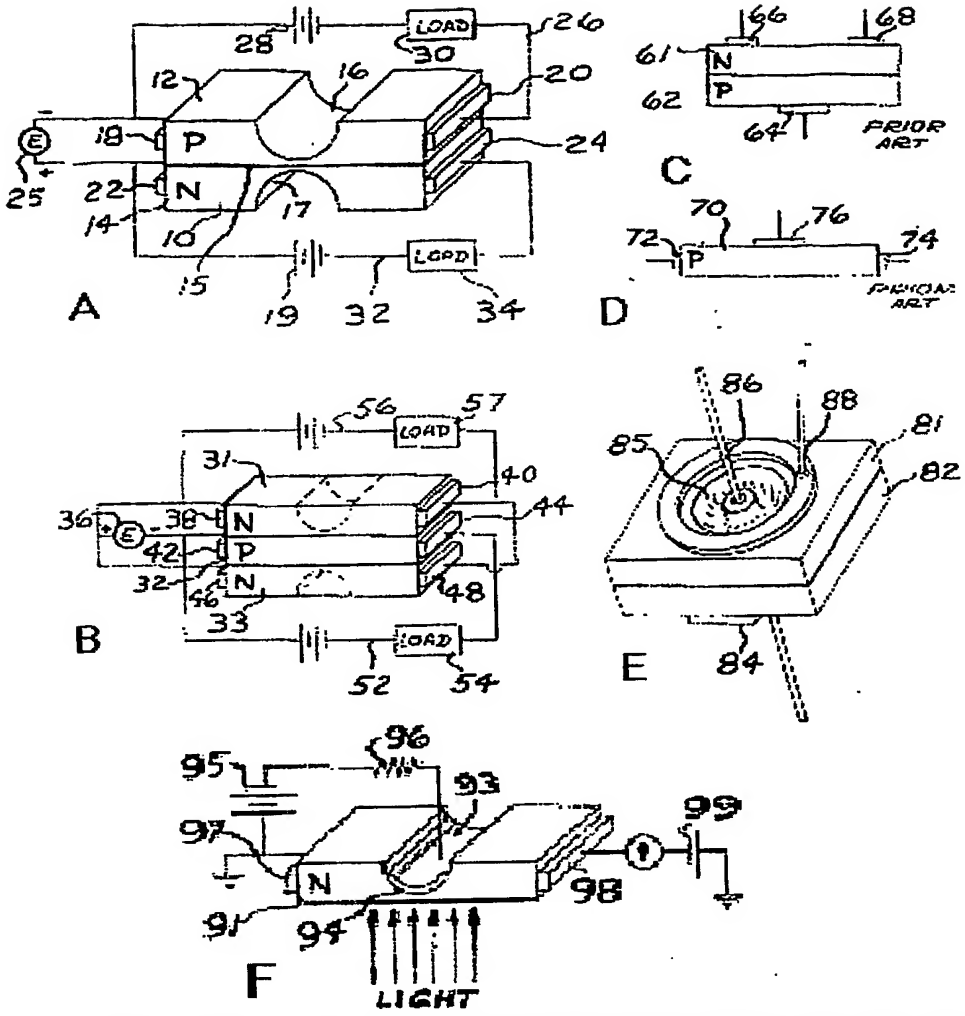


Fig.23: Device structure which can be used as optical sensor, according to [28].

cally designed to provide outputs indicative of the incoming light's colour (although, most likely, it will inherently present an intrinsic efficiency dependent on wavelength). Secondly, the structure of the device clearly shows that the channel region is indented inside the bulk crystal (the quasi-cylindrical moat in which electrode 93 is situated), most probably as a result of intentional etching of the bulk crystal. As it will be seen in the next sections, neither of our proposed structures will have any etched indentation/depression in the channel region.

The second patent of interest [29] deals with a photosensitive device again based on a JFET-type of structure: a diffused *n* region forms a channel and a *p-n* junction with a semiconductor body, thus having a depletion layer incident thereto which imparts a given resistance to the channel. The diffusion depth of the diffused region is selected so that the depletion layer extends to the surface of the device in the absence of applied light to the device. The device also required separate source and drain contact regions for supplying and removing current as well as for allowing light to fall unto the channel region and thus modulate its resistance. The device is claimed to be capable of large changes in channel resistance by application of relatively small amount of light energy.

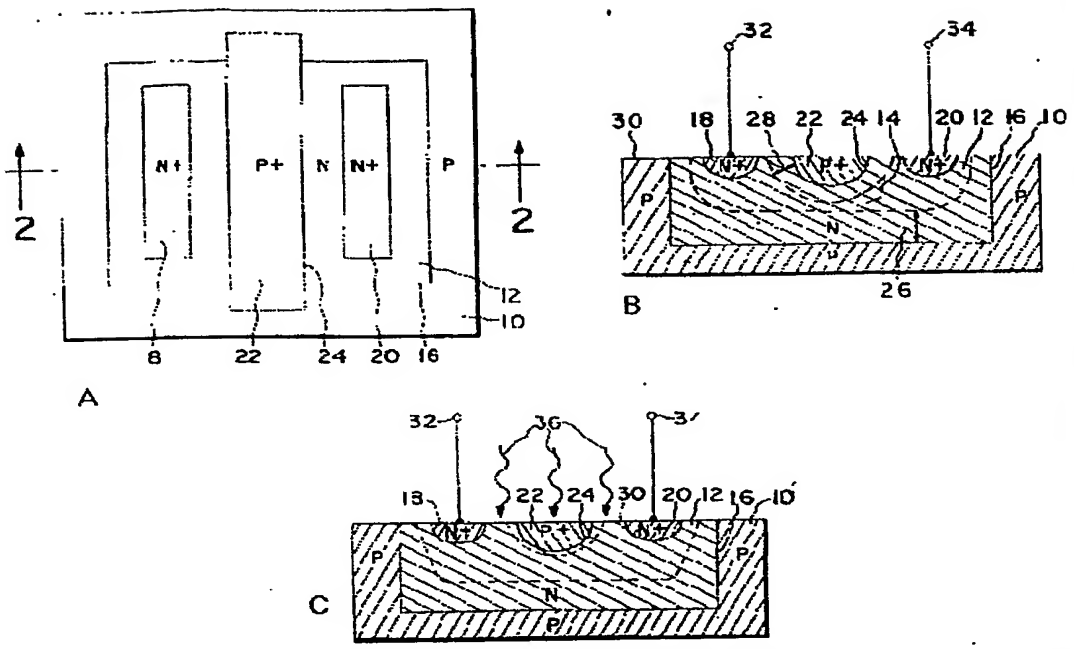


Fig.24: Structure of a FET photosensor intended to be used as photochopper [29]: A) Layout drawing (top view); B) and C) Cross-sections of the device structure without, and with applied light, respectively.

The purpose of this invention is to provide a simple, reproducible sensor, which provides a large change of resistance with modest change of illumination. There is no external bias applied to the *p-n* junction but the device approaches a pinch–off condition because of the internally generated (built-in) voltage of the gate-channel *p+n* junction. The conductance of the channel is modulated by applying light that alters the normally pinched-off space charge region and this in turn modulates the channel conductance through which current passes by varying the cross sectional area of the conductivity path. This device has a very high off- to on-resistance ratio (R_{OFF}/R_{ON}) and such a change is attainable at relative low illumination levels. However, this advantageous feature is employed to obtain a chopper or modulating device in which the drain current is modulated according to the light intensity variation.

Drawing A of Fig.24 is a plan view of this photosensitive device and an elevation sectional view taken along the lines 2-2 in drawing A is presented in drawing 2B, while drawing C shows the effect of incident light on the invented device. This device has a structure very similar to one of our embodiments (see next section), and the photoconductivity modulation is again clearly specified in the patent. However, this patent does not have any colour-related sensing function, just an overall optical one, and which is utilized for photo-chopping/modulation proportionally with the light variation, not for optical or colour detection/imaging purposes.

J.M. Shannon is another inventor that uses JFETs for a solid-state image sensor [30]. The main claim of his invention is an improved solid-state imaging device for operation in the charge storage mode providing higher signal-to-noise ratio. Fig.25 details some important elements of this patent, showing that the inventor modified the classical structure of JFET by using an annular gate for the JFET. When a suitable voltage pulse is applied to the gate (i.e. across the gate-substrate *p-n* junction), an annular depletion region will extend from the gate junction completely blocking the channel between the common source and each of the drains. When the gate voltage is removed, the depletion regions continue to persist during a frame period, except for their slow discharge due to dark current

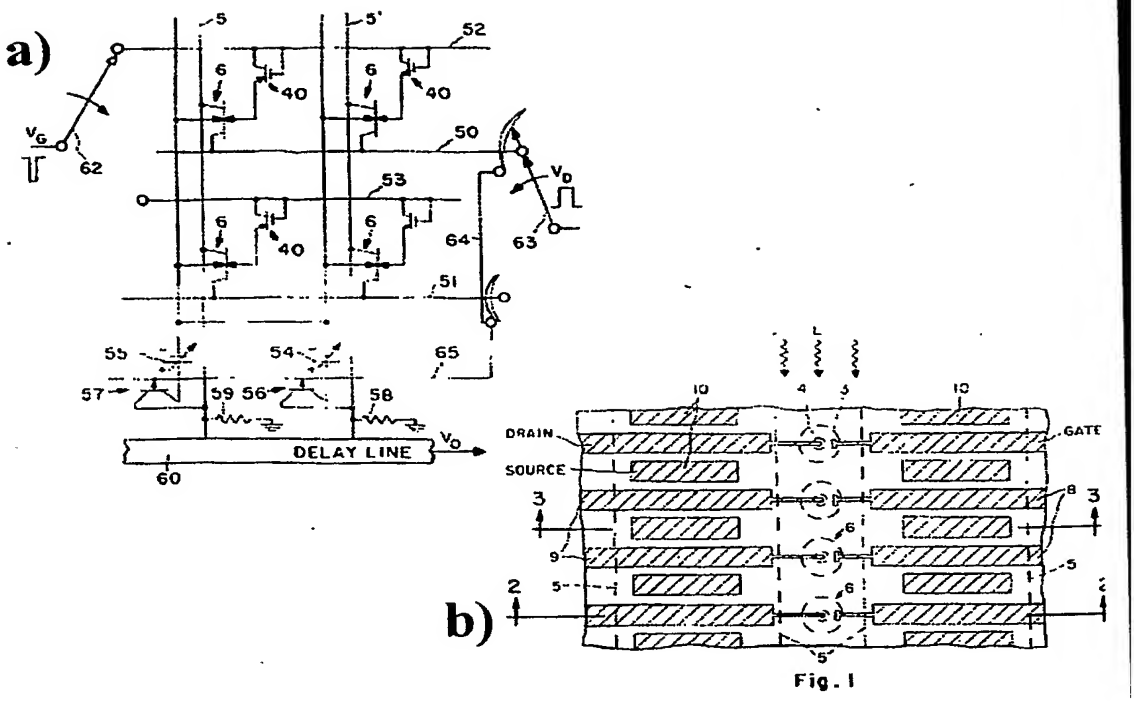


Fig. 1

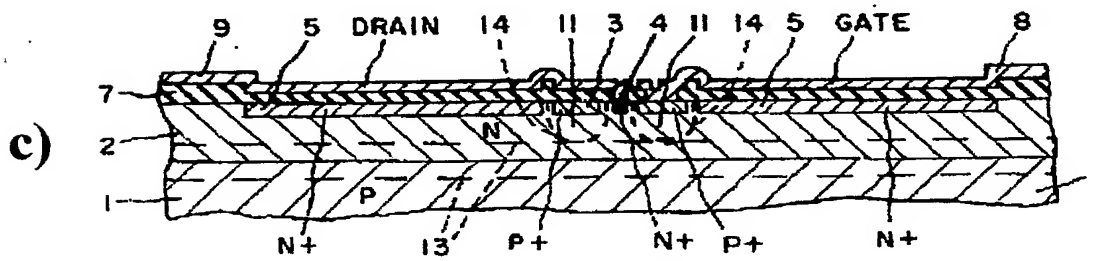


Fig. 2

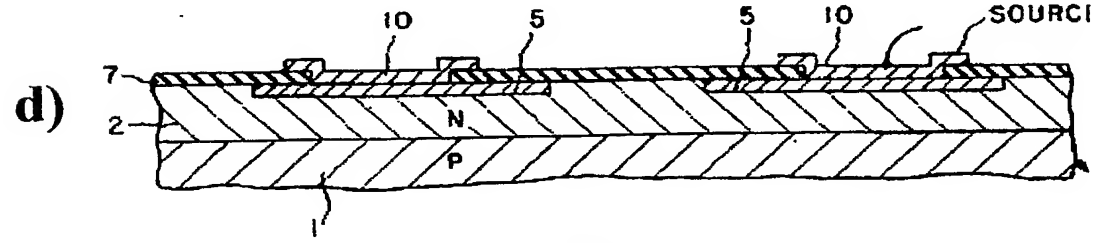


Fig. 3

Fig.25: Patented imaging array based on JFET optical sensors [30]:
a) The linear array of elements; b) Top view of device layout;
c) Cross-sectional view of (b) along line 2-2; d) Cross-sectional view of (b) along line 3-3.

leakage. To interrogate any image element, a voltage pulse is applied to the drain of that element. This can be done at any time and is nondestructive. With no incident radiation the channel of any element exhibits a high impedance and the output signal from that element will be small. Radiation falling on that image element between interrogations will cause the stored charge to leak off at a rate proportional to the radiation intensity and the resistance of the channel reduces accordingly.

From this mode of operation one can immediately notice a major disadvantage of this device: the dependence of the output signal on radiation intensity, i.e. if the light intensity is low or inexistent then the gate diode is not discharged and no signal can be read. This device, just like the one in the previous patent, is specifically suitable for applications in imaging arrays and also has a structure similar to some of our embodiments, with the exception of the annular gate. However, it also has the same important shortcoming that does not qualifiy it as close to the topic of our claims: it does not aim at distinguishing various colours, it serves only as an overall light intensity sensor.

2.2.2.3- SIT-based sensors

Later, Jun-ichi Nishizawa proposed a different imaging sensor using a similar basic principle but with an improved detection method, namely a back-illuminated sensor using an SIT device within its internal structure [31]. The back illuminated type SIT image sensor operates in the electron depletion storing mode (see below for more explanations on various possible storage modes). The sensing principle of this device presented schematically in Fig.26-a is to have a photosensitive region (the n+p junctions 21-23) where there exists an intense electric field. This field allows the photogenerated carriers to flow into the floating region, set at the surface of n+ Source region 25 from where the read-out SIT (n+ Drain 23, n+ Source 25, p+ Gate 26 and n– channel 24) transfers the charge in the floating storage region buried in n+ 23. The stored holes lower the potential barrier height for electrons in the n+ Drain 23, resulting in flowing out of electrons from this region towards the transparent electrode. In the read-out process, the reverse gate bias voltage applied on the p+ Gate 26 returns to 0 V. The read-out process is finished by the electrons in the surface n+ Source 25 flowing into the positively self-biased n+ Drain 23 through the n– channel 24. The stored voltage proportional to the optical input is detected through the sense amplifier transistor Q

Fig.26-b illustrates a SIT-based memory cell, proposed in the same patent, in which the memory function is enabled by a floating storage region set at the surface of the substrate. The device works as follows: when a certain reverse bias voltage (the negative bias voltage) is applied on the word line, the channel region is completely pinched-off by this reverse bias voltage, thus establishing a potential barrier in the channel. On the other hand, when the word line is set at the zero gate bias condition, mobile carriers (electrons) appear in the channel, thus establishing the conducting state (the ON state). If at this moment a positive voltage V_o is applied on the bit line, electrons from the n^+ region flow into the bit line, thus storing the positive voltage Vo on the storage capacitor. This leads to a depletion of electrons in the n^+ region; therefore, this operation mode is called the *carrier depletion-storing mode*. In this mode, the reverse bias voltage between the n^+ floating region and the p^+ gate region increases with increasing the positive bias voltage V_o (the write-in voltage).

The opposite can also occur: excess electrons to be stored in the n^+ floating region. This operation is called the *carrier accumulation-storing mode*. The SIT memory cell functions in the carrier depletion-storing mode because it is superior to the accumulation one with respect to memory-related performances such as retention characteristics and their temperature dependence or operational tolerance. Moreover, the SIT memory cell, particularly when operating in the carrier depletion-storing mode, is capable of storing analogue as well as binary digital information.

The main claim of this invention is to provide a semiconductor image sensor in which the SIT serves as a read-out or refresh transistor. Consequently, the SIT serves auxiliary purposes and is NOT used as the active optical sensing device, let alone as a colour sensor. Another important remark is that this is a backside-illuminated sensor, method which –as it will be seen in the subsequent sections- we shall not employ in our proposed devices.

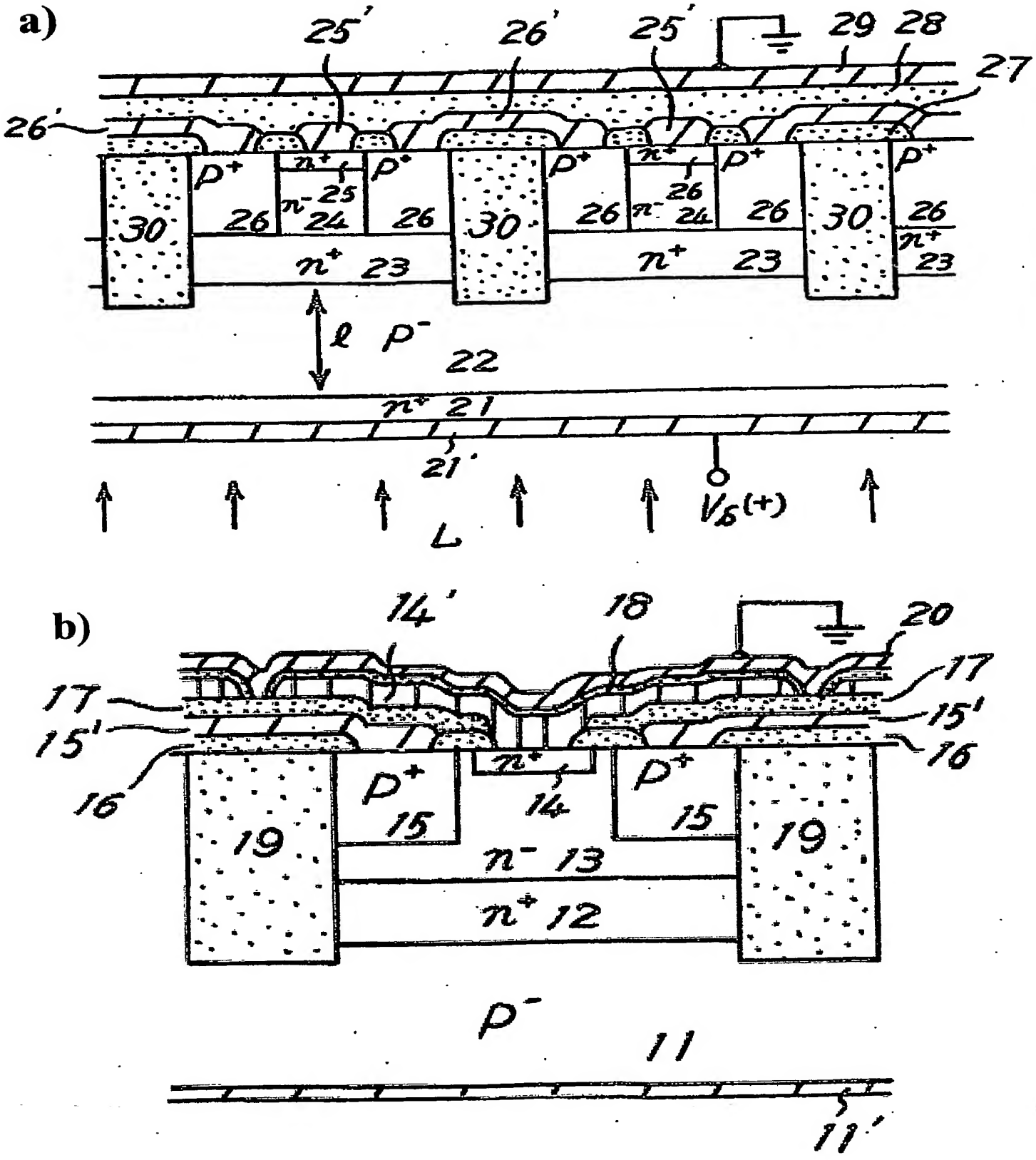


Fig.26: a) Image sensor with memory capability due to a floating storage region set at the surface of the substrate; b) SIT-based memory cell with a floating storage region set at the surface of the substrate (region 14) [31].

Another family of SIT-based device invented by Nishizawa [32] is a high sensitivity semiconductor photoelectric converter like that shown in figure 27C provided by the buried and electrically isolated gate p^+ regions 3 (no electrode is formed to contact this gate region). Therefore, the gate region 3 can be used as a carrier storage region, the substrate 1 is used as the source, and the n^+ region 5 serves as the drain of the SIT, respectively. The spacing interval of the p^+ gate 3 mesh is selected so that the depletion layers due to the built-in potential at the *pn* junctions sufficiently overlap each other, thus providing a sufficiently high potential barrier within the channel region (n^- regions 2 & 4). This results in a non-saturating I-V characteristic that enables an easy enlargement (amplification) of the output current simply by increasing the drain voltage. The correlations between the thicknesses and doping concentrations of the gate, channel and drain regions determine the wavelengths of the light to be detected.

Fig.27 also shows some other relevant patent drawings emphasizing several important structural types of such SIT-based photodetectors. More specifically, the structure in fig. 27D has some important advantages: easy manufacturability, and is suited especially for normal type operation in which the substrate 1 is used as the drain region. The structure in fig. 27E is effective to reduce the gate capacitance because the gate region is reduced in size, so that such structure is most suitable for the detection of weak light. Figure 27F schematically shows a lateral structure, in which current electrode regions are formed in the same principal surface to allow a lateral flow of charge carriers. The operation principle is very simple: optically generated minority carriers are stored in the gate region 3 to control the potential thereof. The resulting holes are stored in the $p+$ type gate region 3 which has a lower potential for the holes, to thereby bias this gate region forwardly. That is, a bias voltage is produced between the gate region and the channel region, which is the sum of the built-in potential (reverse bias) and the electromotive force (forward bias) produced as a result of irradiation by light. This electromotive force is determined by the amount of absorbed light, or in other words, by the amount of electric charge stored in the gate region and the gate capacitance. In accordance with an increase in the amount of irradiated light, the forward gate bias increases and thus gradually diminishes the overall reverse bias applied unto the gate, resulting in shifting the characteristic output I-V curves of the device, as shown in Fig.27B for a SIT photo-transistor with its channel region sufficiently pinched off at zero gate bias (i.e. no illumination). The non-saturating I-V characteristic of this SIT structure observed in figure 27B also enables enlargement of the output current simply by increasing the drain voltage

A high-speed and high sensitivity image pick-up device can thus be obtained by integrating a multiplicity of such SIT-based photoelectric converters. A switching transistor may be merged in the gate region of each photo-electric converter element to enhance the operation speed of the image pick-up device.

The devices in this invention are based on a SIT structure designed so that its series resistance from the source region to the intrinsic gate (the region in which the drain current is substantially controlled) is very small, and thus it exhibits a large transconductance. The impurity concentration of the channel region is selected of low value and the width of the channel region is selected small so that the channel region can be pinched off in the region 14 by the depletion layer extending from the gate (even without any external bias applied unto the gate, just with the depleted region arising from the built-in potential of the gate junction), so as to form an intrinsic gate of a potential barrier type. Also, the gate length is selected short to provide very small series resistance.

The height of this potential barrier produced in the intrinsic gate region can be controlled by either the gate or the drain potentials, and this enables the device to exhibit a non-saturating type of I-V characteristic. The proposed SIT has an additional convenient feature, namely that its gate capacitance can be made very small due to the very small gate length, so that it is suitable for high-speed and low power dissipation operation.

Integrating this photoconverter on the same chip with other circuitry elements can constitute an image pick-up device which requires no application of high voltage or no provision of vacuum. Accordingly, other imaging solutions, which employ semiconductor charge transfer devices (charge coupled devices = CCDs) had been proposed previously. Such charge transfer devices have the advantages of a simple structure and a high packing density. However, the electric charge which forms the output signal is comprised of photogenerated carriers subsequently stored in a MOS capacitor structure. Therefore, if the amount of light irradiated on the device is not intense enough, the electric

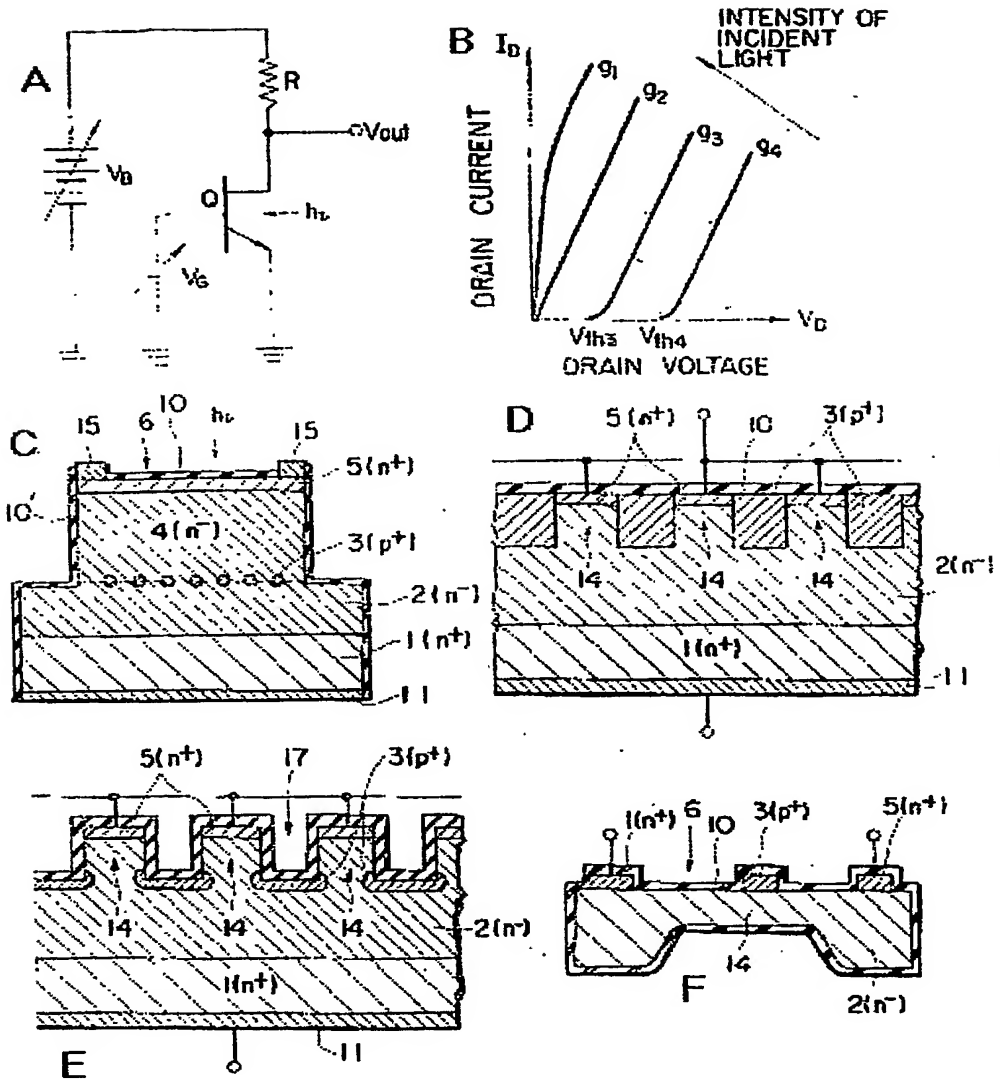


Fig.27: SIT-based semiconductor photoelectric converter [32]: A) circuit diagram; B) I-V characteristic of the photodetector; C) Cross-sectional view of the embedded-gate type structure; D) Cross-sectional view of the surface-gate type of structure; E) Cross-sectional view of a recessed-gate type of structure; F) Cross-sectional view of a lateral-gate type of structure.

charge which is stored will be small. Therefore, it is typically not possible to obtain a large signal with such devices if the light is weak. Furthermore, leakage of the stored electric charge often occurs when it is being transferred inside the CCD during its normal functioning. Similarly, when the *p-n* junction at the source region of a MOS transistor is used as a photodiode the same problems related to sensitivity to light will appear, just like as in the case of charge transfer devices.

In contrast, when light is irradiated onto any of Nishizawa's SIT-based photoconverters shown in Fig.27, electron-hole pair generation occurs (in principle anywhere within the low doped regions 2 and/or 14). The resulting positive holes are stored in the *p* type gate region 3 which has a lower

potential for the holes, thereby forwardly biasing this gate region. That is, a bias voltage is produced between the gate region and the channel region 14, which is the sum of the built-in potential (reverse bias) and the electromotive force (forward bias) produced as a result of irradiation by light. This electromotive force is determined by the amount of absorbed light, or in other words, by the amount of electric charge stored in the gate region and the gate capacitance. Any variation of the gate potential will therefore be translated ultimately in a modulation of the potential barrier across the channel region, and thus induce a strong variation of the drain current, in accordance with the intensity variation of the irradiated light (by default, in the absence of light, there is no drain current if the channel is pinched off, as mentioned above).

From all the structures presented above, those in Fig.26-D and –E resemble to some extent the FCT devices that will be proposed later, whereas the one in Fig.27-F is similar to the FET-based colour sensors which we shall introduce in the subsequent sections. Nevertheless, there are major differences between these structures and those which we shall propose. Namely, this patent shows clearly three important key aspects of the patented devices:

1) SIT-based structures can be used for light sensing and the patented devices clearly are indicated to provide output dependent/proportional to the intensity of incident light;
2) No colour sensing or any other wavelength-related capability is described or claimed.
3) The internal mechanism of gate potential barrier modulation due to charge accumulation in proportion with the amount of irradiated light can be used for an inherent amplification mechanism that does not require any external components but is intrinsic to the sensor (SIT structure) itself, especially if default channel pinch-off can be achieved. This can be related to the conductivity modulation of the channel, but is NOT specifically mentioned as such, and – even more importantly– does NOT rely on photoconductivity-based effects.

2.2.2.4- Other related structures

Another search was again carried out, using the same key words, for **Published Application (AppFT)** patents between years 2001-2003. For "Junction Field Transistor "and "color sensor" no DOCUMENT was found; however, for "Junction Field Transistor "**or** "color sensor" 403 proposed patents. The most significant ones are briefly detailed in this section but all deal with various types of structures that are only partly related either to a real Si-based JFET structure or to colour sensing.

Several patents [33,34] describe devices that are essentially MOS-, not JFET-based, and which are intended for usage only as power semiconductor devices, not for optical or colour sensing. A similar device is a power JFET [35] which has, however, a few similarities to the SIT/FCT-based structures. The device, shown in Fig.28, is claimed to be suitable for a high reverse voltage while at the same time exhibiting low static loses under forward–bias. As it can be seen from Fig.28, the JFET 100 contains a drain contact region (n^+) 41 connected through a drain electrode 40 disposed at the bottom of the device and an inner region (n^-) 13 disposed above the drain contact region and a control region (p^+) 31 disposed above the inner region. A gate electrode 30 is disposed above the control region. A source contact region (n^+) 21 connected through a source electrode 20 disposed in the right part at the top of the device.

In the forward-biasing situation the drift (bulk resistance) for the electric current decreases considerably because of the high doping in the first connecting region (n-doped) 22 and at the same time has no disadvantageous effects on the reverse-biasing behavior because the second connecting region(p-doped) 32 has, for this purpose, an approximately identical doping concentration with region 22, but with a opposite conductivity type. These influences will be reciprocally compensated for one another in the event of a high reverse voltage value.

In this case, both connecting regions 22 and 32 are completely depleted, i.e. there are no longer any free charge carriers existing. The equipotential lines of the electric field then run practically parallel to bottom surface 11. As a result, in the reverse-biasing situation, there is no difference in behaviour from a junction field-effect transistor without any connecting regions. At the same time, however, the static ON-state losses relative to an occupied area in the semiconductor region 10 are considerably reduced by virtue of the more highly doped first connecting region 22. From here the possibility of realizing the junction field-effect transistor 100 with a reduced space requirement.

The junction field-effect transistor 100 can be changed over between an ON and an OFF state by a control potential present at the gate electrode 30. A control potential effecting changeover to the off state causes a channel zone 70, which is situated within the source contact region 21 and the outer part 223 of the connecting region 22, to be completely pinched off or covered by space charge zones of p-n junctions. As a result, the channel zone 70 becomes impassable to the electric current. If the control region (p^+) 31 and the outer part 323 of the second connecting region (p-doped) 32 are projected perpendicularly to the bottom surface 11 of the semiconductor region 10 into a common plane, then the two projections partly overlap. The channel region 70 lies exactly in the region of the overlap. Space charge zones (=depletion layer zones) which bound the channel zone form at p-n junctions between the outer part of the second connecting region 32 and the source contact region and also between the control region and the outer part of the first connecting region. The extent of the space charge zones and thus the current flow can be influenced by a control potential present at the second connecting region and the control region.

An advantage is one in which the gate electrode makes ohmic contact both with the control region and with the second connecting region. This opens up the possibility of influencing the current flow and also the field distribution by a single control potential present at the common gate electrode.

However, despite the trench-based structure (similar to some extent with one of the SIT-based devices to be proposed by us) it is clear that the functioning principle of the device as well as its applications (again power-control related) are completely differently from our devices and their field of colour-sensing applications. Moreover, this JFET can be at least partially composed of a semiconductor material that has an energy band gap of at least 2 eV. The authors preferred SiC for all the semiconductors regions as this material is particularly well suited for such power semiconductor applications. This is due to the extremely low intrinsic charge carrier concentration, the very low material specific ON-state losses, and a higher breakdown voltage in comparison with Si.

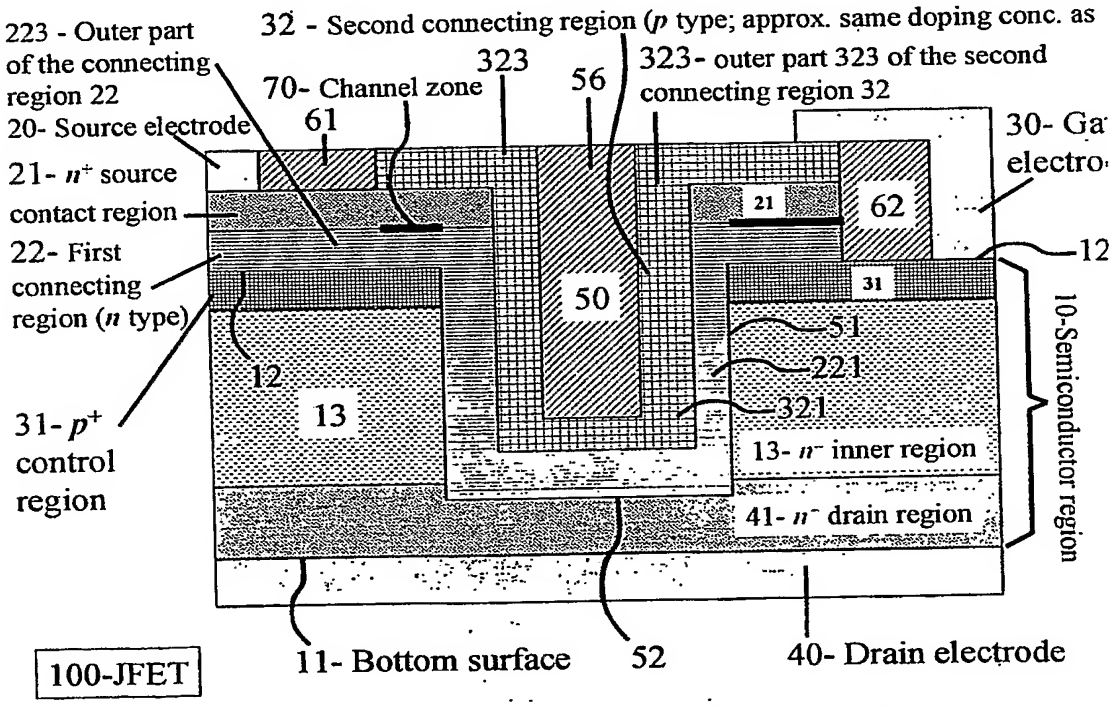


Fig.28: Cross-sectional view of a novel field-effect transistor [35].

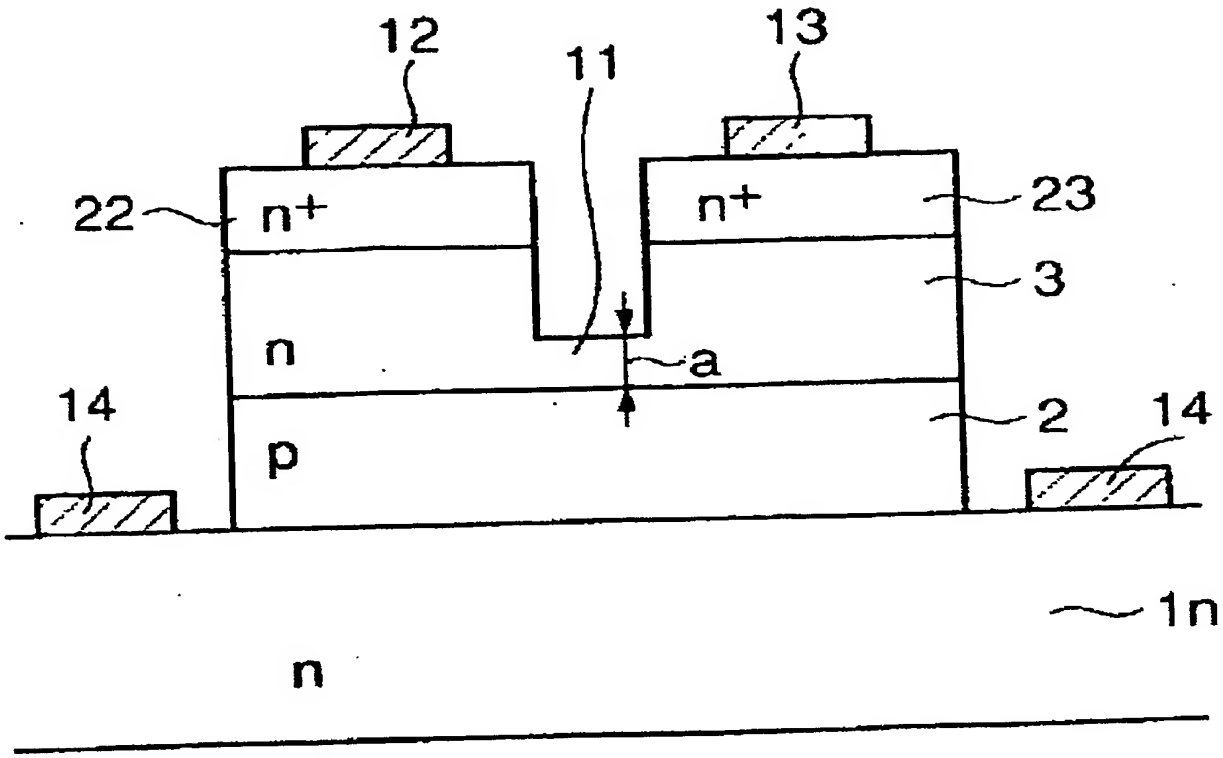


Fig.29: SiC-based Horizontal JFET [36].

Finally, a transversal JFET is shown in Fig.29 but this device is also realized in SiC. The device comprises of an *n*-type SiC substrate (1n), a *p*-type SiC film (2) formed on the right face of the *n*-type SiC substrate, an *n*-type SiC film (3), including a channel region (11), formed in the *p*-type SiC film, source and drain regions (n^+) (22, 23) formed on the n-type SiC film separately on both sides of the channel region respectively, and a gate electrode (14) in contact with the *n*-type SiC substrate (1n).

If a reverse bias voltage is applied to a normal JFET from a gate electrode to a *p-n* junction provided on a side portion of a channel region through which carriers are passing, a depletion layer will be spreading from the *p-n* junction to the channel region, thus controlling the conductance of the channel region for performing operations such as switching. In a "transverse" JFET, carriers move in parallel with an element face in the channel region (perpendicular on top surface of device). For the purpose of convenience, therefore, it is assumed that the carriers for the channel are electrons and hence the channel region is an *n*-type impurity region in the following description, while a *p*-type impurity region, as a matter of course, may alternatively form the channel region.

A voltage is applied in the following manner in response to whether the JFET is normally ON or normally OFF: in the normally ON JFET, the gate voltage is varied from negative (OFF) to positive (ON), whereas in the normally off JFET the gate voltage is varied from zero (OFF) to positive (ON).

When the gate potential is zero, the junction depletion layer, formed between the *p*-type SiC film (2) and the *n*-type SiC film (3) due to the built-in potential, blocks the channel region. Therefore, a normally off transverse JFET can be obtained and can be employed for controlling a power machine without taking countermeasures against breakdown of the gate circuit or the like. Further, power consumption can be reduced in the ON-state, and influence by dispersion of the impurity concentration of the channel region or the like can be avoided.

The authors assert that an advantage of the present invention is employing an n-type SiC substrate which will promote a transverse JFET of uniform quality suitable for a high-power semiconductor-switching element excellent in withstanding voltage and high-speed. Furthermore, it is possible to obtain a transverse JFET capable of suppressing currents leaking from source and channel regions to a first SiC film and prevent any reduction of the amplification factor.

Again, just like in the previous case, the device is only similar to some extent to the devices which we will propose. Furthermore, the material of choice is once more SiC, not Si. In fact, any

devices based on/realized in materials other than Si were plentiful in the documents found after the searches carried out in the previous sections. It is now clear, we hope, that such patents and devices, are totally irrelevant for the purpose of our invention and for this reason they were not even taken into consideration. If any doubts persist, these will be cleared after analyzing the next section, which introduces the devices proposed by us.

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Patent 5,965,875.
http://www.dpreview.com/news/0202/02021101foveonx3.asp then click "Technical Overview"
=> http://www.dpreview.com/news/0202/02021102foveonx3tech.asp

2.4- Proposed structures to be patented

This section will deal with presenting the JFET-, SIT- and FCT- based structures intended for usage as colour sensors. The proposed Patent Title is: **"Colour sensors based on (J)FET structures"**, and the authors are Poenar Daniel Puiu and Mihaela Carp.

2.4.1- Abstract

Colour sensing devices use the light absorption dependence on wavelength as it penetrates through the semiconductor material in which such devices are fabricated, namely Si in this particular case. The internal structure of these devices is mostly based on Field Effect Transistor (FET) structures, especially Junction Field Effect Transistor (JFET) ones, in order to achieve three-colour sensing in a single device that delivers multiple outputs carrying the necessary colour information. Various such sensors are proposed either as large-area stand-alone discrete devices, or as pixels. In this latter case, each sensing device is as small as is technologically possible, and used as an elementary three-colour sensing unit in complex imaging arrays made of a multitude of such identical units. Such an imaging array would deliver RGB signals extracted from the colour information provided in each pixel in the same location.

2.4.2- Background of the invention

2.4.2.1- Field of the invention

The present invention relates to colour sensing, separation and imaging in active (J)FET-based structures which can be used either as stand-alone discrete devices or as active pixels in a complex imaging array. The proposed devices use the (J)FET-based structures to detect carriers photogenerated at different depths due to the different depth penetration and absorption of light of different wavelengths in silicon (Si). Various types of such (J)FET devices are proposed, e,g, using (J)FET structures with either horizontally-oriented channels (i.e. realized with vertically stacked junctions) or vertically-oriented channels.

In detail, the proposed devices can be catalogued in the following type categories:

A) JFET-based (horizontal channel):

A.1) BULK channel (with/without buried layer);

A.1.1) Single (stand-alone) device ;

A.1.2) Imaging *array* based on JFET photosensors

A.2) SURFACE channel

A.2.1) Stand-alone device with either 'normal' structure, i.e. same junction depth for Source (S) and Drain (D) regions, or with different junction depths for each of the S, D & Gate (G) regions;

A.2.2) Imaging device providing simultaneous multiple outputs at collection (current measurement) regions and electrodes;

A.2.3) Stand-alone device & imaging *array* based on a structure with regions of different junction depths (both JFET & MOS).

A.3) 'Triple' JFET (combination of both bulk & surface channels) devices:

a) Compact (G_i=D_{i+1});b.1) Separate channels and independent terminals;

b.2) Separate channels and independent terminals - etched delineation;b.3) Separate channels and common source;b.4) Separate channels with common source & common gate;

B) FCT-based (*vertical* channel)

B.1) BULK channel

B.1.1) Basic structure (stand-alone device)

B.1.2) FCT-based colour sensing *array*

For brevity, whenever convenient, a certain type of proposed colour sensor will be henceforth be distinguished by using the abbreviation code of this classification, e.g. 'JFET-based devices with a surface channel, used as stand-alone devices with similar or different junction depths' will be briefly referred to as 'type A.2.1 devices'.

The largest majority of the proposed devices are JFET-based, and typically employ two junctions to achieve discrimination of three primary colours (R-G-B) at the same location. However, a

few described types achieve not a colorimetric but a rather spectrometric type of colour discrimination of various hues (wavelength ranges) in different locations, whereas other types of devices do employ multijunction structures, although still remaining JFET-based. Finally, there are also proposed devices which exhibit a spectral response that is electrically adjustable by means of an applied potential on a control terminal.

2.4.2.2- Description of related art

All the previous sections and the Figures therein detailed thoroughly the devices based on CCD, bipolar or triple-well structures encountered both in existing literature sources and in previously awarded patents. In other cases (e.g. the JFET-based devices detailed in the U.S. patents No.s 2,993,998, 3,366,802 and 3,721,839, respectively, as well as the SIT-based imaging sensors described in the U.S. patents No.s 4,377,817 and 4,427,990), no colour sensing or discrimination is obtained but only information related to light intensity is provided by the described devices. Finally, a very large number of patented devices that were found in our patent search are only slightly related to our devices due to their JFET- or SIT/FCT-related structure, but they are either used in a totally different manner (e.g. as power devices for electric power control purposes) and as such are inappropriate for colour sensing and/or imaging, or they are realized in other materials (like SiC or compound semiconductors) so that are not of interest for us.

It is the object of the present invention to provide various types of colour sensing devices based on (J)FET structures realized in silicon (Si) either as stand-alone discrete devices or as elementary pixels in complex imaging arrays. However, it may be envisaged that analogous embodiments may be realized in compound semiconductors by adopting the necessary technological and structural changes.

The applications of such colour sensing devices (or arrays), as it was described in the first section, can be multiple, ranging from biochemistry and medicine to food industry and optoelectronics.

2.4.3- Summary of the invention

The present invention is directed to a family of devices in which colour sensing is achieved by taking advantage of (J)FET- or SIT/FCT-based structures. They are intended to be realized mainly in Si, although a profesional well versed in the art may derive similar devices for other materials (e.g. GaAs) by using the proposed structures as initial starting points and correspondingly changing them to accommodate for the inherent material changes that may call for new (or modified) structural features that allow the embodiment of the same operational principle but in a different form (e.g. by using a Schottky junction as gate in an GaAs FET device instead of a diffused junction that can play the role of the gate region in Si).

The first and most important type of proposed devices (A.1), also uses the concept of vertically stacked junctions to act as photodiodes for necessary photogeneration and separation of carriers that ultimately provide the colour discrimination signals, in a manner similar to that described in U.S. Patent 5,965,875. Just as in other embodiments presented in detail in the previous sections (e.g. U.S. Patents 5,965,875, 4,520,381 and 5,883,421), it does not need any polymer filters or separate detectors placed at distinct locations. The first feature allows to avoid any polymer-related processing or reliability concerns, whereas the second one prevents aliasing artifacts and ensures smaller colour sensing units which enable more compact integrated realizations of complex arrays, i.e. of increased imaging resolution. However, unlike all the other devices realized in the past and previously reported, there are unique and crucial features characteristic only to our devices, not met in any of the previously published or patented embodiments. Explicitly, all our proposed devices of the A.1 type employ or have the following distinctive and unique features:

1) A structure with only **two** vertically stacked junctions (not three as in some of the previously mentioned Patents) used both as photodiodes for the active part of the sensor as well as for delineating the middle (channel) region of the device. This middle (channel) region is therefore situated **within the bulk** of the device, at a depth and with a width dictated by the depths at which the top and bottom gate junctions, respectively, are realized;
2) The two above mentioned vertically stacked junctions are used to make up JFET devices and used for JFET operation, i.e. their structure and utilization is not based exclusively only on detection of the currents photogenerated in the stacked photodiodes. Additionally to this

photodetection mechanism, the proposed JFET structures of A.1 type and their operation mode also imply that the middle (channel) region will:

a. Have a current passing **along** it (along the *y* direction, parallel with that of the wafer's surface, within the interior of that specific region), i.e. the channel region is contacted at its ends by two strongly doped contact regions at the surface of the wafer that act as Source (S) and Drain (D), respectively;
b. Absorb 'middle' wavelength range photons only (i.e. situated approximately in the green-yellow ranges of the visible spectrum), as the short and long wavelength photons (violet-blue and orange-red, respectively) will be absorbed and cause photogeneration in the depletion regions of the top and bottom gate junctions, respectively;
c. Use not only photogeneration to create necessary photocurrents in depleted regions that extend over certain portions of the channel (most important when the device has its quiescent operating point placed immediately at or slightly above pinch-off so that the default drain-to-source darkness current is effectively zero; $I_{DS}=0$), but also **photoconductivity modulation 35 of the channel due to photogenerated carriers.** This latter effect, unexploited for colour sensing in previous embodiments, is especially important when a non-zero quiescent drain-to-source darkness current occurs by applying a default drain-to-source voltage bias (V_{DS}), so that illumination with photons of certain wavelengths (i.e. that are absorbed at depth values corresponding to the vertical extent of the channel, typically in the green-yellow part of the spectrum) will effectively modulate this I_{DS} current. The existence of both these effects will allow the usage of the JFET in a larger multitude of working regimes, depending on the type of connections and biases applied unto its terminals;

3) A structure with **two** separate gate regions, including the related strongly doped diffused parts necessary for contacting them, and the necessary contact terminals, respectively. The two gates will be distinguished as the top and bottom gate, respectively, corresponding to the depth of their junction with the channel region. Thus, the top gate junction will serve for the photodetection of the short (violet-blue) wavelengths that are easily absorbed in the most superficial part of the silicon wafer, whereas the bottom one will be used for the photodetection of the long (orange-red) wavelengths that penetrate deep and are absorbed in the wide depletion region generated by this channel-bottom gate photodiode. Of course, obtaining the classical standard JFET structure with a single gate terminal can be easily obtained by short-circuiting together the two gate terminals of our device(s) and therefore applying the same bias voltage to the semiconductor regions to which these terminals are connected. However, as it will be seen in the next section, optimal colour detection needs the application of different potentials on each of these gates, and therefore a structure in which each of these regions can be separately contacted is more advantageous for colour sensing purposes;

The A.1 type of devices can be envisaged and realized as either stand-alone discrete devices, or as miniaturized pixels, i.e. elementary three-colour sensing units in complex imaging arrays which (after subsequent necessary amplification and signal processing) deliver RGB signals extracted from the colour information provided in each pixel in the same location.

Similarly, all our proposed devices of the A.2 type employ or have their own distinctive and unique features, as follows:

1) Unlike the A.1 type of devices in which the channel is located in the bulk of the semiconductor, the A.2 type of devices utilizes **a superficial channel**, i.e. situated in the immediate vicinity of the semiconductor surface;
2) Due to the inherent JFET mode of operation and the necessary biasing voltages it requires, it is more advantageous to adapt the A.2.1 type of structures for sensing colour in a rather spectrometric approach, i.e. various spectral responses will be obtained at different locations of the sensor, and the resulting signals will be picked up by local collecting regions inserted along the superficial channel region;
3) As a direct consequence of adding the above mentioned adapting feature (local collecting regions along the superficial channel region) to the initial A.2.1 type of structures, the A.2.2 type of devices will result, which due to their inherent structure are intrinsically configured to

simultaneously provide multiple output signals. Such devices can be employed in spectrometers and spectrographs, and the advantage brought by this specific A.2.2 type (i.e. superficial channel JFET with multiple colour sensing terminals) of embodiment is that it may offer a very good resolution due to the extreme simplicity of its structure, limited (at least theoretically) only by the photolithographic resolution used in its practical fabrication. The proposed A.2.2 type of device can be used either as a stand-alone realization, or as a unit in an imaging array of more such elements;

4) Another possibility of modifying the A.2.1 type of devices is by purposedly designing each of the S, G & D region with a specific junction depth, tailored for optimal absorption of only a certain wavelength range of the visible spectrum. This results in the A.2.3 type of structure, but which can be used optimally rather as a stand-alone device.

The A3 type of devices combine both the previous types, i.e. they comprise of both bulk and channel regions, and more versions of such devices are proposed. In this case, the details of each device version and their features are as follows:

1) Epitaxial growth is used as the main method to obtain the transistors, and the necessity for deep diffusion regions for contacting deeper situated epitaxial or buried regions is replaced by using diffusion after trench etching, followed by refilling of that trench;
2) Vertical stacking of more JFET structures, such that the region that forms the top gate of one transistor is also used at the same time to form in it the channel, drain and source of the upper JFET transistor. This allows for a more detailed chromatic sensing of the influences prodiced by various wavelength ranges, recommending this device for more accurate chromatic and/or spectrometric-like type of colour detection;
3) Vertical stacking of more JFET structures, but in which each channel region does not act as gate for another transistor and is separated clearly from the other transistors by strongly doped gate regions which enclose each transistor of the triple unit. The following various versions were proposed:
    a) With separate channels and independent terminals for all the transistors;
    b) With separate channels and independent terminals for all the transistors, but with delineation of each transistor by etching of the epitaxial region in which it is formed in an island pattern;
    c) With separate channels but common source;
    d) With separate channels and both common source and common gate.

Finally, B-type devices have other distinguishing features, as follows:

1) Just as for the standard SIT, the sensor employs a vertical channel structure, with deep and strongly doped lateral trenches used as gate regions. (As mentioned above, the need for deep diffusions for such regions can be replaced by using polySi-refilled trenches). However, in contrast with the typical SIT/FCT devices employed in electrical power control, the proposed device for colour sensing will not work in forward bias, but will reverse bias the anode (A)-cathode (K) junction.
2) As a direct consequence of the above feature, B-type devices will develop simultaneously two depleted regions (from the anode and from the gate junctions with the cathode region, respectively) that compete with each other for the limited existing space in the bulk of the semiconductor. Therefore, the potential applied unto the gate may be used to control the extent to which the anode depleted region will develop in depth, and thus control the spectral response of this junction.
3) The gate junction in the previous embodiments was realized by etching the substrate and then carefully performing Selective Epitaxial Growth (SEG) to fill in this trench with strongly doped epitaxial silicon. In contrast to this approach, we propose instead a simpler, easier and more efficient alternative: after etching, polysilicon is deposited uniformly unto all the walls of the trench. If desired, the polysilicon can fill in the trench and then –if necessary- planarized using Chemo-Mechanical-Polishing (CMP). If the polysilicon layer was deposited using *in-situ* doping, after a short thermal cycle, the dopant will diffuse into the trench walls of the substrate, thus creating the desired gate junctions.

4) A simpler version of B-type device may employ only a single top anode-gate region by realizing deep and strongly doped gate regions merged with the anode region. This latter region is realized as a shallow junction, but with a depth much smaller than that of the laterally neighbouring deep gate regions. This results in a SIT-like photodiode structure with an uneven junction profile, in which the same phenomenon of competing depleting regions occurs: the deep and stronger doped regions will faster develop the depleted region laterally and therefore impose restrictions upon the extent to which the superficial anode region can extend its own depleted region. Consequently, the penetration depth of the anode depleted region will be greatly enhanced, and depending on the applied anode-gate potential, which results in a voltage-controlled spectral characteristic.

Just as in the previous cases, the B-type devices can be realized and employed as either stand-alone discrete devices, or as miniaturized pixels in imaging arrays.

A better understanding of each proposed device, its structure, operation and functioning, characteristics and advantages will be obtained by reference to the following section and their detailed descriptions and drawings which set forth illustrative embodiments in which the concepts of the invention are utilized.

2.4.4- Brief description of the drawings

Fig. **31** is a cross-sectional drawing illustrating the simplified schematic structure of an A.1.1 type of colour sensing device, i.e. a JFET-based structure with a horizontal channel in the bulk of the semiconductor.

Fig. **32** illustrates in detail the operation of an A.1.1 type of device as a colour sensor.

Fig. **33** illustrates in detail the operation as a colour sensor of a modified A.1.1 type of device that employs a buried layer under the channel region, of approximately the same dimensions with the top gate region.

Fig. **34-a** illustrates how the A.1.1 JFET-based devices can be employed to build the simplest and most compact colour imaging array with a minimal number of regions and terminal, for an increased resolution in a given area.

Fig. **34-b** illustrates a more complex imaging array that also employs A.1.1 JFET-based colour sensing devices as elementary pixels, but in which each separate part has now been fully delineated and contacted, e.g. both the bottom and top gates can be independently contacted, and each pixel has its own buried layer region. The thick dotted line shows that it is possible to simplify somewhat this design by merging together the bottom gate regions of the pixels along one row in a single unique region.

Fig. **35** is a cross-sectional drawing illustrating the structure of a stand-alone JFET-based colour sensing device with a superficial channel.

Fig. **36** is an approximate 3D isometric and cross-sectional drawing illustrating the structure of a JFET-based colour sensing device with a superficial channel modified by adding shallow strongly doped regions for providing simultaneous multiple outputs at collection (current measurement) electrodes.

Fig.**37** presents various graphs illustrating the absorption of light in junctions of different depths and with depletion widths of various values:

a) Absorption of light in junctions of constant depth (D= 1μm) but with different depleted region widths *w*

b) Light absorption in shallow junctions of different depth and with different depleted region widths *w*, for light with wavelength λ=400 nm;

c) Light absorption in medium-depth junctions with different depleted region widths *w*, for light with wavelength λ =550 nm;

d) Light absorption in deep junctions with different depleted region widths *w*, for light with wavelength λ =700 nm

Fig.**38** illustrates qualitatively an example of spectrometric separation of light into multiple narrow-passbands.

Fig. **39** presents various cross-sectional drawing illustrating structures of A.2.3 types of devices:

a) A stand-alone JFET-based colour sensing device with S, G and D regions having each a different junction depth optimized for photogeneration and collection of carriers of different wavelengths. Shallow $p+$ regions and corresponding metalization contacts were inserted in the channel region to shortcircuit the gate junction and thus achieve a depletion region width of constant and minimal value along the entire gate junction length.

b) A cross-sectional drawing illustrating an A.2.3 type of colour sensing device with S, G and D regions of different junction depths, in which the gate depletion region width of constant and minimal value along the entire gate junction length is achieved by inserting a $p+$ region shallowly buried immediately under the channel region.

c) A cross-sectional drawing illustrating an A.2.3 colour sensing device with S, G and D regions of different junction depths and with a $p+$ region shallowly buried immediately under the channel region, but which was modified by adding an MOS gate made of a thin gate oxide and a transparent control gate terminal.

d) Top view of a layout drawing for the A.2.3 colour sensor of the previous type shown in Fig.39-b (with S, G and D regions of different junction depths) when used as a stand-alone colour sensor.

Fig. **40** describes the generic structure of a triple JFET structure for multi-band colour sensing. This A3 type of device results from combining together in a single structure both JFET-based colour sensing devices previously introduced: with bulk (A.1.1 type) and surface (A.2.3 or A.2.1) channels, respectively. The region which is used to act as top gate for a JFET transistor is also used to act as channel region for the transistor stacked above, and in which the corresponding S & D terminals are placed (hence the resulting notation G_i=D_{i+1}).
(***Note:*** *due to lack of space in Fig.40, some light components, their related phenomena and the resulting effects were depicted to take place outside the active/illuminated region* ***19****, although, obviously, in practice this is not the case*).

Fig. **41** schematically shows the concept of another A3 type of JFET-based colour sensing device, with separate channels and having all the S, G, D terminals of each of the stacked JFET transistors independent/separate and accessible. In this case the channels are not placed in regions directly adjacent one to another (as was for the device in Fig.40), but are separated by strongly doped gate regions:

a) The cross-sectional structure of the device, highlighting its regions;

b) A possible layout representation of the device. The previous cross-sectional drawing was considered along line A-A'.

Fig. **42** shows other A3 devices, resulted from various modifications brought to the structures presented in Fig.41:

a) A cross-sectional drawing illustrating the schematic conceptual structure of an A3 device similar to that shown in Fig.41-a, but in which each transistor and its channel-including regions have been delineated by anisotropic etching. This allows for the same strongly doped contact diffusions to take place simultaneously and thus simplify the device processing;

b) A cross-sectional drawing illustrating the structure of an A3 device similar to that shown in Fig.41-a, but with a single, common source region and corresponding terminal, respectively, for all the transistors;

c) A possible layout representation of the device shown previously in drawing (a). The previous cross-sectional drawing was considered along line A-A'.

Fig. **43** is representing another device resulted from the modification of the A3 device shown in Fig.41-a:

a) A possible layout representation of the device;

b) Cross-sectional drawing of the device along line B-B'. The cross-sectional drawing of the device along line A-A' is the same with that shown ion Fig.42-b.

Fig. **44** illustrates the FCT-based colour sensing device with a bulk vertical channel:

a) A cross-sectional drawing showing the structure of a stand-alone device entirely realized in monocrystalline Si;

b) An approximate 3D isometric and cross-sectional drawing illustrating the operation and the schematic circuitry required for proper biasing and functioning structure of a stand-alone device with the gate realized by tremch etching and filling with polysilicon;

c) A cross-sectional drawing of the structure with merged A & G regions, resulting effectively in a SIT/FCT-like photodiode with nonuniform top junction profile;
d) An approximate 3D isometric and cross-sectional drawing illustrating the structure of an FCT-based colour sensing array;

2.4.5- Detailed description of the invention

It is well known that the penetration and absorption of light in a semiconductor, in this case silicon as most important exponent of this family, is dependent on the light wavelength. Namely, short wavelength light (the violet-blue range of the visible spectrum) is quickly and strongly absorbed in silicon and therefore does not penetrate to great depths, whereas long wavelengths (orange-red) are only slowly absorbed and therefore penetrate to a much greater depth and require a significantly wider region for complete absorption. Consequently, considering the exact dependence of the Si extinction coefficient k on wavelength λ one can calculate the necessary junction depths and depletion region widths to achieve good colour spectral separation in a three-junction type of device, as indicated previously in Fig.3 of Section 1.2.1 and Fig.12 in section 1.2.3 of this document, respectively. Our junction depth and corresponding depletion region width values indicated both in Fig.12 and in Table 1 are close to, but nevertheless different from, the values of x_{j1}=0.2 μm and w_1=0.3 μm, x_{j2}=0.5...0.6 μm and w_2=1 μm, and x_{j3}=2 μm and w_3≈1 μm, respectively, which can be extracted from the U.S. Patent No. 5,965,875 of Merill et al. These differences are probably due to:

a) The different spectral selectivities which probably were initially targeted by Merill et al., due to their digital imaging targeted applications;
b) The restriction imposed by the applied CMOS-compatible triple-well technology, as well as
c) The different reverse bias values (different from those used in our initial calculation) that might be applied across each of the photodetecting junction, limited by the inherent constraints imposed by the employed structure.

All these differences may result in different spectral sensitivities of the devices. For this particular case of the newly proposed devices, we are interested to use the sensors both for imaging or non-imaging colour-sensing. This may comprise similar possible applications, like digital imaging, but also spectrometric applications (for a few of the proposed structures). Moreover, we are interested that our sensors could be used for imaging and/or colour sensing for medical or bio/chemical applications, in which a very wide range of wavelengths could be sensed with a single type of structure. Thus, the upper junction for our proposed devices is much shallower than in the device proposed by Miller et al.,, so as to extend the sensing capability of our device as much as possible into the violet and near-UV range. The middle channel region in our devices should have a responsivity peak around 550 nm, so as to imitate the photopic response of the human eye. Lastly, the bottom junction should be quite deep, so as to maximize the response in the wavelength range 700...800 nm or even beyond, so that the spectral response of this junction could also gather as much light as possible with wavelengths in the near-IR. Ultimately, of course, the designer may change the device parameters as to optimize a desired application, and this is especially true for the spectrometric-like sensing devices for which the designer should conceive the various parameters of interest as most convenient for a achieving a desired response shape.

The first type of proposed structures are A.1 type devices, i.e. JFET-based colour sensors which have only TWO junctions that delineate in the bulk of the semiconductor a middle portion that forms the 'channel' of the device. Fig.31 shows the schematic structure of such a device and its component elements. It can be easily seen that no triple-well structure is necessary, although, if so desired by those skilled in the art, one can easily envisage the modification of this structure and replace the middle epitaxial region with a diffused one, resulting in a triple-diffused structure similar to that of Merill et al. However, because the epi-grown method is much more practically convenient to realize, we shall apply such an implementation method whenever it is applicable for a specific device.

Fig.31 represents a device with a n-type channel, and the same type of n-type channel JFET devices will be discussed in almost all the subsequent Figures, excepting the case where multiple JFETS are stacked in a single device. If necessary, the structures in this Figure and all the subsequent Figures can be quickly re-drawn as, and the subsequent explanations related to them can be easily and

equally applied to, structures in which the doping types of all the regions are reversed (i.e. *p*-type regions become *n*-type and viceversa) and the polarities of the applied bias voltages (where applicable) are correspondingly changed appropriately to allow for the correct operation of the device so that its functioning remains identically the same.

Fig.31 shows the schematic structure of a possible generic embodiment version for an A.1 type device. The following distinct regions can be identified:

- A low doped (e.g. approx. 10^{15} cm^{-3}) substrate region **1** (*p*-type for an *n*-channel device, as shown in Fig.31);
- A strongly doped (e.g. approx. 10^{19} cm^{-3}) region **2**, of the same doping type as the said substrate, realized on the backside of the wafer in order to contact efficiently the substrate region and thus to allow the substrate region to efficiently act as bottom gate region;
- A region **3** of comparable or lower concentration (e.g. approx. $10^{14}...10^{15}$ cm^{-3}) and opposite doping type compared to those of the said substrate, epitaxially grown to a thickness of e.g. 5...10 μm on top of the said substrate, depending on the wavelength range to be absorbed in the middle channel region **5** and on the values of biases to be applied and the operating regimes in which the device would be used;
- A top region **4** of the same doping as the substrate, shallowly diffused (e.g. 0.2...1 μm) and of a large surface doping concentration (e.g. approx. 10^{19} cm^{-3}), which forms the top gate region. Again, the depth of the junction **13** formed by this top region **4** with the epi region **3**, the doping profile of the top region **4** and the reverse bias to be applied on this region may depend on the desired short wavelength range which is desired to be absorbed by the depleted region developed at this junction (not shown in Fig.31);
- Source and drain regions **5** of the same doping as the epitaxial region **3**, but of a large surface doping concentration (e.g. approx. 10^{20} cm^{-3}). The depth of these junctions may be chosen by the designer as a compromise between the requirement of a low series resistance (deep junctions, e.g. 3...4 μm), and that of a smallest possible size (i.e. minimizing lateral diffusion by choosing shallow junction depths of, e.g., 0.5...1 μm) that allows the largest integration density and (if the device is realized as a pixel in an imaging array) thus the greatest resolution for a given technology;
- Metallizations **7**, typically realized using aluminum (Al), which realizes the ohmic contacts with each important semiconductor region of the device and the interconnection to the terminals or pins **8**, **9**, **10**, **11** of the source (S), top gate (G_1), bottom gate (G_1') and drain (D), respectively. These pins or terminals ensure that the device can be connected to external circuitry and/or bias supplies required for the properly functioning of the device. Alternatively, when the device is not a stand-alone discrete embodiment but represents an elementary pixel in a larger and more complex imaging array, the aforementioned metallization routes enable the interconnection of this pixel and its elements to other components of the array, e.g. row and/or column circuitry and/or other (neighbouring) pixels of the same array.

The channel region **5** is defined vertically by the junctions **12** and **13** made by the top (shallow but strongly doped) gate region **4** and the bottom (low doped but thick substrate) gate region **1** with the epitaxial region **3** of opposite doping type. Horizontally it can be considered as stretching from approximately the middle of the source region to the middle of the drain region, respectively. Consequently, this channel region **5** is totally enclosed within the bulk of the semiconductor and it also has the following essential characteristic features:

a) Has a current passing **along** it (along the ***y*** direction, parallel with that of the wafer's surface), between the two strongly doped contact regions **6** contacted by the Source (S) **8** and Drain (D) **11**, respectively;
b) Absorbs 'middle' wavelength range photons only (i.e. situated approximately in the green-yellow ranges of the visible spectrum), as the short and long wavelength photons (violet-blue and orange-red, respectively) will be absorbed and cause photogeneration in the depletion regions of the top and bottom gate junctions, respectively;
c) Uses not only photogeneration to create photocurrents in depleted regions that extend over a certain portion of the channel **5** (most important when the device has its quiescent operating point placed immediately at or slightly above pinch-off so that the default drain-to-source darkness current is effectively zero; I_{DS}=0), but also **photoconductivity modulation 35 of the**

channel 5 due to photogenerated carriers within this channel 5. This latter effect, unexploited for colour sensing in previous embodiments, is especially important when a non-zero quiescent drain-to-source darkness current occurs by applying a default drain-to-source voltage bias (V_{DS}), so that illumination with photons of certain wavelengths (i.e. that are absorbed at depth values corresponding to the vertical extent of the channel, typically in the green-yellow part of the spectrum) will effectively modulate this I_{DS} current. The existence of both these effects will allow the usage of the JFET in a larger multitude of working regimes, depending on the type of connections and biases applied unto its terminals.

It must be highlighted that Fig.31 presents only one possible embodiment. Another embodiment equivalent in functioning and purpose can be obtained if, for instance, the strongly doped region **2** is actually the substrate, on top of which the low doped region **1** is realized with the desired thickness as a first epitaxially grown layer, followed by the growth of region **3** of opposite doping, which can be realized without interrupting the epitaxial growth procedure or breaking the low vacuum, just by switching on and off the necessary doping gases. The bottom gate (G_1') contact **10** and its corresponding metallization **7** can still be realized on the backside of the wafer, as shown in Fig.31, or could be transferred on the top side of the wafer. In the latter case, a supplementary deeply diffused and strongly doped region **14** will be required in order to achieve the desired contacting from the front side of the wafer, as it will be seen in Fig.32. Despite this supplementary step, the overall processing is not lengthened as compared to the previous version shown in Fig.31, and the front-side contacting is much more convenient for devices to be used as elementary pixels in complex imaging arrays.

Fig.32 details the operation of a JFET-based colour sensor of the A.1 type. For simplicity, most of the notations already introduced in Fig.31 have not been repeated again here, and only the significant new elements are specifically numbered and explained as follows.

- The substrate region **1** can have a low or a high doping concentration, but in either case it is now contacted from the top side for the device shown in Fig.32. This contact is realized using a deep diffusion **14** of high surface concentration (e.g. approx. $10^{19}...10^{20}$ cm^{-3}), and of the same type of doping as the substrate region **1**. The choice for a substrate of either low or a high doping concentration depends on the spectral range of light desired to be detected by the bottom junction **12** between the substrate and the subsequent epi layer of opposite doping type, as is explained more detailed below.
- Depleted regions **15** and **16** will form at the junctions **12, 13** and **17** between the epi region **3** and the bottom and top gates and their contact regions **4, 1,** and **14**, respectively. As is well known, these depleted regions develop due to the bias potentials applied on the S, G_1, G_1' and D terminals (**8, 9, 10, 11**), according to the typical operation of a JFET:
  - The potential **81** applied unto the S terminal **8** is usually the ground potential (V_S=0),
  - The D terminal **11** is connected at a positive voltage V_D **111**. This determines the onset of a the D-to-S current I_{DS0} **18** flowing through the device, with a value determined by the magnitude of the applied D potential V_D **111**, the electrical and geometrical parameters of the channel region **5**, and the value of any external current limiting resistor that might be connected in series with the D supply bias **111**. The index zero in the abbreviation I_{DS0} used for this current **18** shows that we refer to the default current flowing through the device in a stationary regime in darkness, i.e. without the influence of any incident light falling unto the device. Under these circumstances, the indications of two current meters **82** and **112** connected in series with the D & S terminals **8** and **11** will be identical in values, but of opposite signs.
  - The bottom gate G_1' terminal **10** is connected to a potential V_{G1}' **101** (which can be variable between 0 to extremely negative values, i.e. $|V_{G1}'|>V_D$), and
  - The top gate G_1 terminal **9** can be either connected to a small negative potential V_{G1} **91** (shown in Fig.32 with broken lines) or, even better, short-circuited to the S terminal **8** and thus connected to the same ground potential **81** ($V_{G1}=V_S=0$), as joining the S terminal **8** with the top gate G_1 terminal **9**.

It can be noticed that Fig.32 depicts the case of a strongly negative potential **101** applied to the bottom gate G_1' terminal **10**, whereas no reverse biasing is applied for the top gate junction ($V_{G1}=V_S=0$). This results in top and bottom depleted regions **16** and **15** of different thicknesses: the bottom depleted region **15** is much wider due to the strong

reverse bias applied across the junctions **12** and **17** between the epi region and the bottom gate G_1' region **1** and its contact region **14**, respectively. However, the width of both depleted regions **16** and **15** increases significantly from the S terminal **8** towards the D terminal **11** because the reverse potentials that are locally applied along the junctions are not constant but increase from the S to the D, exactly because of the different potential values applied unto these two different terminals. In any case, as again is well known, the extents of the depletion regions **15** and **16** within the channel region **5** under the top gate G_1 region **4** narrow the cross-section of the path through which the I_{DS0} current **18** flows (especially in the immediate neighbourhood of the D terminal **11**, as is also shown in Fig.32). In standard JFETs, this enables a small variation in the gate potential to be translated into an amplified variation of the I_{DS0} current **18**.

- As shown in Fig.32, only a part of the entire device is exposed to the incoming light **20**, namely in the so-called active area **19** only. The rest of the device is considered to be opaque, i.e. the incident light **20** does not penetrate and influence other regions. This can be achieved, e.g., by shielding the device with a thin layer of metal after almost the entire processing sequence is carried out, and then defining the active area **19** by opening a window and removing the shielding metal only in this region **19**.
- The extent of the depletion regions **15** and **16** determine the spectral responses of each photosensitive region. The detailed spectral behaviour of each photosensing region is as follows:
    - The short-wavelength, i.e. violet-blue (B), component **201** of the incident light **20**, is absorbed in the depletion region **16** of the most superficial junction **13** developed between the epi region **3** and the top gate region **4** of opposite doping types, within the active area **19**. Consequently, the depth of the top gate junction **13** and the width w_B **21** of the top depletion region **16** determine the shape of the spectral response of the photodiode formed by junction **13**. The depth of the top gate junction **13** can be controlled by varying the processing parameters that lead to formation of this region **4** during the device fabrication sequence, whereas the width of the top depletion region **16** depends both on technological parameters (e.g. the doping levels of the regions **3** and **4** between which the junction **13** is formed) and on the reverse bias applied unto the top gate G_1 terminal **9**. Even if no such reverse bias is applied (as is the case depicted in Fig.32), the built-in bias developed across the junction **13** provides a depleted region of sufficient width to ensure a response peak in the violet-blue part of the visible range. Orientative values for depth of the top gate junction **13** and the width of the top depletion region **16** are 0.05 μm and 0.2 μm, respectively, as was indicated previously in Fig.12. More accurately, when the B component **201** of the incident light **20** is absorbed in the depletion region **16** of the top gate region **4**, it will lead to the photogeneration pairs of free carriers **22**, which will instantly be separated by the internal field within the depleted region **16**. The carriers of one charge type (negative, i.e. electrons, for the case depicted in Fig.32) will reach the epi region **3**, where they give rise to a small photocurrent **181** which contributes to the default I_{DS0} current **18**. The other carriers reach the top gate region **4** where they give rise to a 'violet-blue' photocurrent I_B **23** which can be detected by a current meter **92** connected in series with the top gate G_1 terminal **9**. The fact that the top depletion region **16** has an increasing width from the source terminal **8** to the drain terminal **9**, instead of a constant width along the channel **5**, can influence the spectral responsivity for this depletion region **16** but does not compromise its operation for photodetection. The spectral response will probably be covering a wider wavelength range than expected (extending more into the cyan-green part of the visible spectrum), but the effect can be controlled to some extent by appropriately designing the length of the top gate region **4** (and thus of the channel region **5**, too), the doping levels of the regions **3** and **4** between which the junction **13** is formed, and by choosing the bias values applied unto the top gate G_1 terminal **9** and the D terminal **9**.

- The green-yellow (G) component **202** of the incident visible light **20** should be absorbed in the middle part of the devices, namely in the part of the channel region **5** delimited by the top and bottom depleted regions **16** and **15** and within the active area **19**, as shown in Fig.32. The absorption of these light quanta also determines the photogeneration of pairs of free carriers (not drawn in Fig.32). However, inside the channel region **5** there is no depleted region to separate these photogenerated carriers and the rapid removal of the minority carriers from the epi region **3** is not an efficient process due to two factors: first, the diffusion-based movement of these minority carriers cannot proceed along the shortest route to the nearest depleted region because of the influence exerted by the applied V_{DS} potential. Secondly, strong recombination with the majority carriers may take place along the distance to the edges to the nearest depleted region, and this factor is much accentuated by the previous factor, i.e. the applied V_{DS} potential lengthens considerably the path necessarily followed by the minority carriers, thus increasing their recombination probability. Therefore, carriers photogenerated inside the channel region **5** delimited by the top and bottom depleted regions **16** and **15** contribute much more significantly to another local effect, namely **photoconductivity modulation 35** in the channel region **5**. This effect, on its turn, correspondingly modulates the drain-to-source current, changing its value from the default one I_{DS0} **18**. Hence, this variation will affect both the current meters **82** and **112** connected to the source and drain terminals **8** and **11**, respectively. A better differentiation between the darkness vs. under-illumination indications can be made when the device has its quiescent operating point placed immediately at or just slightly above pinch-off so that the default drain-to-source darkness current is very small, i.e. close to zero: $I_{DS} \approx 0$. In this case, the photoinduced channel conductivity variation is immediately and clearer noticed as a change in the drain-to-source current at an increased value very different from the close-to-zero one corresponding to the background pinched-off stationary state. However, one must bear in mind that the indication shown by the source current meter **82** is the composed resultant of variations due to all the wavelengths components absorbed in various portions of the device, as was already mentioned previously with the contribution **181** due to half of the B photogenerated carriers, and as it will be immediately be presented about the contribution **182** due to half of the carriers photogenerated by the long-wavelength red (R) component **203** of the incident light **20**.
- The long-wavelength red (R) component **203** of the incident light **20** is absorbed in the depletion region **15** of the junction **12** developed between the epi region **3** and bottom gate region **1** of opposite doping types. The width w_R **24** of this depletion region **15** should be quite large, in order to allow for the necessary deep and wide absorption region required to detect properly the R light, as it was previously presented in Fig.12. Just as with the top gate junction, the width w_R **24** of this depletion region **15** is controlled by both technological parameters (thickness and doping level of the epi region **3**, doping level of the *p* substrate region **1**) and electrical ones (the bias potentials **111** and **101** applied unto the D & G_1' terminals **11** and **10**, respectively). Moreover, one can now distinguish the two parts w_{Rn} **241** and w_{Rp} **242** of the width w_R **24** of this depletion region **15** which are distributed across the epi region **3** and the substrate **1**. Different implementation alternatives are thus possible, depending on the intended result and the technological limitations. One such version can have the epi region **3** much more strongly doped than the substrate **1**, e.g. $10^{15}...10^{16}$ cm^{-3} compared to 10^{14} cm^{-3}, respectively. In this case one would have $w_{Rp} >> w_{Rn}$ and that effectively makes $w_{Rn} \approx 0$. This means that $w_{Rp} \approx w_R$, i.e. the entire width w_R **24** of the depletion region **15** extends only in the substrate **1**. The advantage of this version is that the deep penetration of the depletion region into the substrate enables the usage of only a thin (~3...4 μm) epi layer **3** and a not very long diffusion to form the strongly doped contacting region **14**. This shortens the fabrication cycle and also allows for smaller lateral

dimensions, which in turn may allow an increased integration density, and thus a higher resolution (when the device is a pixel in a large complex imaging array). Its disadvantage is that it initially requires expensive low doped wafers and that the higher doping of the channel region may decrease the impact of the photoconductivity modulation effect **35**.

Another alternative is to use a cheaper and more strongly doped substrate **1**, and then grow on it a much less doped epi region **3**. In this case $w_{Rn} >> w_{Rp}$ and $w_{Rp} \approx 0$. This means that $w_{Rn} \approx w_R$, i.e. the entire width w_R **24** of the depletion region **15** extends only in the epi region **3**. This may be beneficial for the photomodulation modulation effect but obviously requires an extremely thick (about 15 μm) epi region **3** in order to provide all the necessary space for the depleted region **15** to extend into. Even if the growth of such a thick epi region **3** does not pose problems related to contamination from the substrate into the epi layer, there still remains a severe drawback: an even deeper diffusion has to be carried out in order to realize the strongly doped contacting region **14**. This will severely limit the resolution which one can attain in imaging arrays, due to the large lateral dimensions required by this diffused region alone. Moreover, the dopant from the substrate may also diffuse into the epi layer and viceversa, resulting in a rather linearly graded bottom junction 12 instead of an abrupt one. Consequently, given all the major drawbacks of this alternative, it is the less attractive for practical implementation.

Finally, a compromise can be found, in which both the epi and the substrate regions **3** and **1**, respectively, have doping levels of comparable concentrations. Consequently, the two parts w_{Rn} **241** and w_{Rp} **242** will be about a half of the total width w_R **24** of the depletion region **15**. Again, just as for the depleted region **16** of the top junction **13**, the width w_R **24** of the depletion region **15** will not be constant along the device but will increase from the source to the drain, due to the applied biasing potentials.

- When the R component **203** of the incident light **20** is absorbed in the depletion region **15** within the active area **19**, it will lead to the photogeneration pairs of free carriers **25**, which will instantly be separated by the internal field within this depleted region **16**. The carriers of one charge type (negative, i.e. electrons, for the case depicted in Fig.32) will reach the epi region **3**, where they form a small photocurrent **182** which contributes to the default I_{DS0} current **18**. The other carriers reach the bottom gate substrate region **1** where they give rise to a 'red' photocurrent I_R **26**. This R photocurrent **26** is collected via the deep and strongly doped contacting region **14** and thus can be detected by a current meter **102** connected in series with the bottom gate G_1' terminal **10**. The fact that the bottom depletion region **15** has an increasing width from the source terminal **8** to the drain terminal **9**, instead of a constant one, will also influence the spectral responsivity but does not compromise its operation as a photodetecting region. The spectral response will be covering a wider wavelength range than expected (extending more into the orange-yellow part of the visible spectrum), but the effect can be controlled to some extent by appropriately designing the length of the top gate region **4** (and thus of the channel region **5**, too), the doping levels of the regions **3** and **1** between which the junction **12** is formed, and by choosing the bias values applied unto the bottom gate G_1' terminal **10** and the D terminal **9**.

In the entire above description of the device's operation, it was implicitly assumed that the current meters **82, 92, 102** and **112** are used to measure the generated photocurrents or the variations arising from photoconductivity modulation, respectively. In other words, it is assumed that the externally applied biases are always constant, and the currents (or their variation) are measured. This is in contrast with the operation that is used for the devices described by Jun-ichi Nishizawa in U.S. Patent No. **4,427,990**, where the photogenerated currents determine a variation of the reverse bias applied unto the gate of his devices, thus resulting in modifications of the I-V curve of the devie, i.e. of the current flowing throught the structure. Although such an operational mode is in principle possible for our devices, too, it is preferable to operate them as described above. This is because

adopting a functioning as for Nishizawa's devices would result in a too complicated spectral dependence of the drain current variation on the wavelength of light. Our proposed operational mode is therefore simpler and more convenient to use for our proposed devices.

Fig.33 shows a similar JFET-based colour sensor structure, but in which a strongly doped buried layer **27** (of the same doping type as the epi region **3**) has been inserted below the top gate region **4**, and slightly wider than the active illuminated region **19**. Its presence will effectively remove one the negative effects described above, namely the possibility to use an equally low doped epi layer **3**. The only disadvantage brought by this alternative is that, if the epi region **3** has now a low doping level, the large width of the bottom depletion region **15** will also automatically imply a wide lateral extension of the same depletion region in its vertical part **15'** as it surrounds the strongly doped contacting region **14**. This means that large distances should be provided on the layout between the regions **14** and **6l**, hence reducing the integration density and the imaging resolution of an array made of such elementary pixels. However, a possible solution to this problem is to simply isolate the region **14** from the rest of the areas by using STI (Silicon Trench Isolation), as is done in the standard high-density CMOS fabrication. In this way, the maximum possible pixel packing density could be achieved.

Finally, if appropriate doping levels are chosen for the epi layer **3**, the top gate region **4**, the buried layer **27** and the substrate **1**, the necessary V_D bias supply value may be decreased (as compared to that used with the device of Fig.32) and thus the nonuniform width of the top depleted region **16** may also be reduced, as shown qualitatively in Fig.33, too.

Just as for the previous version of the colour sensing device shown in Fig.32, the G1 current sensed by the current meter **92** is effectively a 'blue' (B) photocurrent and the G_1' current sensed by the current meter **102** is effectively a 'red' (R) photocurrent. The D current meter **112** will indicate the drain-to-source current, either in its default quiescent (i.e. darkness) value I_{DS0}, or its value altered after illumination due to photoconductivity modulation **35** of the channel region **5**. Consequently, one can easily extract the 'green' (G) response by subtracting the illuminated response value from the quiescent value indicated by the same drain current meter **112**. This can be done either by using a memory function (analog, e.g. using a capacitor, or digital, based on sampling, and then converted to digital form that is then stored in a memory cell), or –simpler- by just always having an identical device used as reference, i.e. which is not exposed at all to the incident light but is totally covered by the aforementioned top shielding metal in which no active area **19** is defined. A simple circuit (again, either analog or digital) can then carry out the necessary subtraction between the two signals. Another alternative possibility is to use the total final current I_{DS}(B+G+R) **27**, namely its value provided under illumination by the S current meter **82** and subtract from it (using a similar subtracting circuit correspondingly adapted to have several inputs) the B and R values provided by the current meters **92** and **102**, respectively, as well as the default value I_{DS0} indicated by the D current meter **102** of a separate, reference sensor.

It is evident that the JFET-based colour sensing devices presented in Figs.31 and 32 can be realized either as stand-alone discrete devices, or as miniaturized elementary pixels in complex imaging arrays.

Fig.34 presents the embodiment of two possible imaging arrays based on the above mentioned A.1.1.a and A.1.1.b type of JFET-based colour sensors presented in Figs.32 and 33. Fig.34-a presents a conceptual drawing representing the first embodiment of such an imaging array based on the colour sensor of type A.1.1 detailed in Fig.31, whereas Fig.34-b shows the most important control signals for such an array. The only main difference from the basic device presented in Fig.31 is that regions **6** now have to be clearly distinguished as sources or drains, not only in terms of functionality (for applying correctly the necessary external biases) but also related to their specific layout. It can be seen that the source regions **6'** are now effectively merged into a single long stripe, whereas the drain regions **6"** are still separate and independent for each transistor, i.e. imaging pixel. Moreover, the source stripes **6'** are common for both their left- and right-hand neighbours, i.e. the same source line S_j can be used when scanning the drains of the transistors of both the columns *j-1* and *j*. More precisely, as it can be seen in the detailed representation pictured in Fig.34-a, the same strongly doped line acts as both the source S_{j-1} for the pixels/transistors to its left (i.e. the transistors with gates $G_{i,j-1}$ and drains

$D_{i,j-1}=D_{i,j-2}$) and the source S_j for the pixels/transistors to its right (i.e. the transistors with gates $G_{i,j}$, and drains $D_{i,j}=D_{i,j+1}$). This means that, during the operation, the drains and sources are alternatively used for both the columns situated to their left- and right-hand sides, respectively. This merging of the elements of neighbouring pixels into a single functional area allows for the greater integration density that enables a better resolution on a given silicon area. As it can be seen in Fig.34-a, the transistors/pixels $T_{i,j}$ are interlaced with each other due to the functional elements they have in common. Fig.35 also presents in more detail (right hand top corner) the exact composition of each transistor in such an array, except for the very first and the last columns, respectively.

Similarly to the source stripes and drain areas, the bottom gate contacting region **14** can be made as a single highly doped stripe, unique either for the entire array, or just for an entire column of the array. This would allow again a greater integration by using a single such element for the entire array/column, and furthermore, such an arrangement is convenient also because this common region can now easily be placed at a safe enough distance from the entire array that would allow the lateral extension of the depleted region **5'** to develop freely.

Both these arrangements (common sources for the left- and right-hand pixel columns and unique or reduced number of bottom gate contacts) result in the most possible compact arrangement, i.e. the one which enables the highest density of pixels and therefore providing the highest possible resolution. The price to be paid for this is a decreased accuracy in estimating the colour information: the red signal, for instance, is extracted from the only one terminal common for the entire array (or for a given column). However, this inaccuracy may not be exceedingly large, given the fact that one can design the control circuitry so that the R signal reading is synchronized with the sequential scanning of the transistors in the array (i.e. the application of the source & drain biases on each pixel) and the influence of the background can be subtracted using a reference ('blind') pixel. Similar considerations can be made for the signal read at the common source lines. Consequently, it will be easy for the signal processing circuit to determine from which pixel of the array belong the instantaneous R, G and B values read from the array at any given moment.

The operation of the array (considered to have M rows and N columns) can be better understood with the help of the signal diagrams shown in Fig.34-b. It can be seen that any source stripe common to the ***j-1*** and ***j*** columns is normally in a high impedance state. It is activated by connecting it to GND potential only during the periods of time necessary to sequentially scan all the transistors in the columns to its left and right. This scanning effectively means that positive pulses Φ_i ($i=1...M$) are applied in sequence unto the drains $V_{D\ i,2k-1}= V_{D\ i,2k}$ that make up the column of $n+$ regions that has at its left and at its right the $G_{i,2k-1}$ and $G_{i,2k}$ columns of gates, respectively. As it can be seen in Fig.34-b, the M drain adressing pulses are applied twice because the first time the left-hand pixels are addressed, whereas the second time, the right-hand ones are selected. This means that the gates in the $G_{i,2k-1}$ column are addressed sequentially and the source line S_{2k-1} (to the left of the $G_{i,2k-1}$ and $D_{i,2k-1}$ gate & drain columns) is connected to the ground during the first set of M drain pulses, whereas while during the second set of M pulses the right-hand $S_{2k}=S_{2k+1}$ source line has $V_S=0$ and the $G_{i,2k}$ gate columns are addressed sequentially. When the drain scanning of all transistors in this column has been completed, the procedure is continued for next column of drain regions $D_{i,2k}= D_{i,2k+1}$. The same source line that was previously active, $S_{2k}=S_{2k+1}$, continues to be kept at $V_S=0$, and another set of $2M$ drain addressing pulses begins to address the next column of drain regions $D_{i,2k}= D_{i,2k+1}$, and so on, so forth. From Fig.34-b it is obvious that during this scanning, an unselected transistor has his source unconnected at GND (a HiZ output from the control circuit addressing the source lines), whereas the drain and gate bias of a selected pixel/transistor take the necessary positive and negative voltages, respectively, only during the application of the corresponding pulses. Therefore, the following phenomena will occur during the short period of applying the selection source, gate & drain pulses:

- Drain current will flow between the source & the drain, which will be modulated due to the photoconductivity modulation determined by the green component of the light incident unto that respective pixel;
- Significant reverse biasing of the top gate region **4** will occur, resulting in developing the previously mentioned depletion region **16**, which ultimately allows to detect, as a gate current, the contribution photogenerated by the violet-blue component of the light incident unto that respective pixel;

- The bottom gate contact **14** allows the collection of the signal which provides the info related to the R component of the light incident unto that respective pixel, even if it is common for the entire array or an entire column. This is because, when the drain pulse is applied unto a pixel, significant reverse bias occurs only **locally** on the bottom gate region **1** in the area immediately beneath and around the selected pixel, as the bottom junction **12** is reversed biased only by applying the drain pulse. This allows for a photogeneration effect much more significant then in the rest of the array/column, where only limited reverse biasing (the default built-in voltage across the junction **12** of the bottom gate region **1** will occur. The contribution for the rest of the array can then be deducted from the overall signal, if it has been read once for every row or frame scanning (in other words, this means that an interval equal with that for reading of a pixel is required between the frame scanning to refresh the background information by reading the output signal(s) at the unbiased common gate and memorizing it/them for further usage in the calculations during the next scanning sequence).

Of course, it has to be highlighted that numerous other array control versions may be possible. For instance, one simplification can be brought if the user does not need to reverse bias the top gate, as the default width of the depletion region **16** at junction **13** due to the built-in electric field of the junction may be sufficient for the desired violet-blue selectivity. In this case, obviously no separate gate signals need to be applied and the same signals which are applied unto the sources will also be applied unto the gate terminals, respectively.

In general speaking, numerous possibilities can be conceived for a most suitable addressing of the array. Such solutions have to be used as the JFET is a "normally-ON" device, unlike most of all the other semiconductor devices (diode, bipolar and MOS transistors) which are typically "normally-OFF". Consequently, solutions must be used in order to allow a true matrix-type of addressing, i.e. that enables a convenient control of an $M \times N$ array with only $M+N$ output lines. This can be achieved, for instance, by adding one or more "normally-OFF" devices to each active pixel photodetector, such as MOS transistors, in a circuit added to each pixel element. This circuit would activate correctly the necessary pixel, according to the selection signals provided by classical matrix-type addressing control circuits, and at the same time should route correctly the collected (and pre-amplified) responses towards the signal processing circuitry that extracts the colour information from the output signals of each pixel. Such a circuit would be designed according to the specificities imposed by both the type of basic photosensing device used in each pixel and the desired structure for the imaging array. In any case, this circuit can be easily added next to each pixel by those skilled in the art by using standard IC design methods, layout and technology.

Another possibility of implementing practically such an imaging array is depicted in Fig.34-c. Here, each pixel has its separate connections for top and bottom gate, and source/drain, respectively. As it can bee seen, the source of one transistor is confounded with the drain for the transistors of the next column, and the bottom gate contact regions **14** can either be separate or –if so desired– be merged into a single line **14'** common for a whole row. The fact that the source of one transistor is confounded with the drain of the transistor in the next column implies that the signal addressing is also slightly different: a zero voltage pulse is applied on the source of the selected pixel, while simultaneously applying a positive pulse on its drain and a negative pulse on its top gate, respectively. Selecting the pixel on the next column means that the $n+$ region **6** which played the role of the drain now becomes the source, and it is brought to zero, while a high positive pulse is applied to its other $n+$ region **6** that is now the drain, and so on. The output circuit delivering the control signals to the array must therefore maintain all the other pixel regions that are not selected into a high impedance (HiZ) state.

It can also be noticed that Fig.34-c depicts a version in which a buried layer is realized beneath the gate region of every pixel, while the substrate is of low doping. Both these measures, as explained above when discussing Fig.33, would determine a large extension of the bottom depleted region **15** only in the substrate, thus enabling the usage of a thin epi region **3**.

Finally, as was mentioned previously, allowing for a separate connection for each and every region of the JFET transistor making up each pixel would require a larger area, the most important contribution being due to the large distance necessary to accommodate the lateral expansion **15'** (see again Fig.33) of the depleted region **15** developed when reverse biasing the junction **17** between the

contact **14/14'** with the bottom gate region **1**. A good solution in minimizing this undesired effect is to isolate entirely the contact region **14/14'** from the rest of the device by using STI (Silicon Trench Insulation) techniques, as highlighted in Fig.34-c, too.

Fig.35 presents another JFET-based device (A.2.1). It can be noticed that, unlike the previous devices shown in Fig.s 31-34, its channel region **5** is placed in an extremely superficial region very close to the surface of the wafer, and is of the opposite type as compared to the surrounding epi region **3**, thus forming with it the junction **41**. This epi region **3** now has the same doping type as the substrate, although in a much lower concentration. In this case, as shown in the Figure, the gate contact would be realized using the highly doped substrate. The bias voltages applied unto each terminal are the same as those used for the devices in Fig.s 31-34, thus leading to the appearance of a default current I_{DS0} **18** flowing through the device. However, unlike the previous devices, the opaque regions **42** are arranged such that light will fall unto different regions of the device. This could ensure photogeneration due to various wavelengths in various regions:

- the violet-blue light will determine photoconductivity modulation **35** the current I_{DS0} **18**, as well as photogeneration in (part of) the depletion region **16** under the channel region **5**;
- the green light will cause photogeneration in (part of) the depletion region **16** under the deeper $n+$ region **6** of the source contact **8**; and
- the red light will cause photogeneration in (part of) the widest extemsion of the depletion region **16** under the deeper $n+$ region **6** of the drain contact **11**.

However, this elementary structure has some serious drawbacks:

- There is a significant lateral extension of the depleted region;
- Nonuniform width of the depletion region **16** under the channel region **5**;Difficulty in collecting the photocurrent along the channel region **5**.

In order to eliminate or minimize all these flaws, various implementations were considered. In a first such embodiment, the simplified concept of Fig. 35 was modified into the new and more practical A.2.2 device structure, which is shown in Fig.36, that addresses specifically the last drawback in the list above. Additionally, the A.2.2 structure in Fig.36 is basically the same with the A.2.1 one of Fig.35 but the disadvantage of a varying width of the depletion region **16** under the channel region **5** is now exploited in an advantageous manner for achieving spectroscopic-like colour sensing. More specifically, the channel region **5** is now extremely long, and is also modified so as to include extremely shallow but strongly doped gate contact regions **29**. These gate contact regions **29** will, however, not be connected to any external biasing source. Due to its considerable length, relatively shallow junction depth and quite low doping concentration (slightly higher, and/or comparable to that of the underlying epi region **3**, but certainly much smaller than the doping of the S & D regions **6**), the channel region **5** will exhibit a very high resistance. This resistance, when measured e.g. with reference to the source contact **8**, will gradually increase towards the drain contact **11**. Therefore, when the positive drain biasing **111** and the negative gate biasing **101** are both applied unto the respective terminals **11** and **10**, two phenomena will occur:

a) A drain-to-source quiescent current I_{DS0} **18** will flow, with its intensity depending on the value of the positive drain biasing **111** and the total resistance of the channel region **5**;
b) The depleted region **16** will also develop, with its width varying from the minimal possible extension value w_{min} **161** to a maximal extension value w_{MAX} **162**. If no gate external bias is applied the former value will be due only to the default built-in potential developed at the junction **46**, whereas the latter one will be dictated exclusively by the positive drain bias supply value **111**.

In other words, due to the high resistance of the channel region **5**, the drain-to-source voltage drop will be distributed uniformly along its length, thus resulting in a smoothly varying width of the depleted region **16**. If the length of the channel region **5** is large enough (i.e.the channel length L_{chan} **51** is much larger than the width l_i **293** of the strongly doped top gate contact regions **29**: $L_{chan} >> l_i$) and the width of the strongly doped top gate contact regions **29** is made as small as possible, then one can easily consider that the width w_i **291** of the depleted region is constant under a certain gate contact element i. This means that photogeneration will take place in the depleted region **16**, but different wavelengths will contribute to this phenomenon under different contact regions **29**. The short light will be most significant for the portion of the depleted region **16** under the contact regions **29** closest

to the source. As one moves from the source towards the substrate along the channel region **5**, a wider and wider light spectrum of wavelengths will contribute to this photogeneration process. Fig 37 presents qualitatively how such a phenomenon occurs, for the generic case of a junction with a depth of 1 μm, and for various depletion region widths. Therefore, one can obtain multiple sharper and narrower spectral responses by manipulating the primary responses that would be collected by each of the gate contact regions **29**, e.g. $I_{\lambda 2-\lambda 1}= a_1 I_1$, $I_{\lambda 3-\lambda 2}= a_2 I_2 - a_1 I_1$, $I_{\lambda 4-\lambda 3}= a_3 I_3 - a_2 I_2$, ... $I_{\lambda(N+1)-\lambda N}= a_N I_N - a_{N-1} I_{N-1}$, with I_i= the current measured/collected at the i^{th} top gate contact region **29**, and λ_1, λ_2,.. λ_N, λ_{N+1}= the wavelengths defining the narrow-band domains desired to be investigated. The multiplication factors a_i represent amplification/attenuation coefficients for the circuits that pick-up and process the corresponding signals collected at each i^{th} region, in order to compensate the unequal magnitude of absorption for each region (as can be seen in Fig.37-a) and thus provide for normalized final response curves. It is obvious that by varying the geometrical dimensions p_i **292** and l_i **293** one can control the type of response, i.e. the values λ_1, λ_2,.. λ_N, λ_{N+1} of the spectral regions desired to be separated. Fig.s 37-b, c and d show the various absorption characteristics typical for various cases of interest, namely they indicate how one can select a certain junction depth and the necessary depletion width to attain a a certain light absorption, and hence detection. It thus becomes clear that this type of device is most suitable not for a colorimetric but for a spectrometric type of measurement, in which numerous narrow pass-band domains within the visible range are isolated and separately examined, as illustrated in Fig.38.

Moreover, two more degrees of freedom for the designer are provided by means of electrical processing of the measured signals, too:

- By varying the value of the total applied positive potential V_{DS} **111**, one can control the *slope* of the depleted region variation from source to drain;
- By varying the value of the bottom gate voltage V_G' **101** one can control the overall width of the depleted region along the entire channel region **5**.

Consequently, adding at these two control ways the possibilities previously described (using a different, and even variable, amplification/attenuation coefficients for the pick-up circuit of each channel, as well as the initial design choice for the parameters p_i **292** and l_i **293**) results in an extremely flexible device, whose spectral characteristics can first be determined by layout design, and secondly can also be electrically controlled to achieve the desired responses.

When light falls unto the active (illuminated) area **19** of the device, it causes photogeneration of free carrier pairs **22** in the depletion region **16** (for simplicity, in Fig.36 only one such pair **22** was represented in a local part of the depleted region **16**). Due to the internal field within the depleted region **16**, these carriers will be easily and extremely rapidly separated. Thus, the hole(s) will form a small substrate current **451** that will contribute to the formation of the total photocurrent **45** which can be sensed by the current meter **102**, whereas the electron(s) will most likely reach the closest contact regions **29**, where it/they could be collected. Nevertheless, it may also be possible that it/they may form a small additional current component **181** contributing to the drain-to-source quiescent current I_{DS0} **18**. Consequently, one should properly design the read-out circuitry connected at the measurement terminals M_i **43**$^{(i)}$ (i=1...N). On one hand, the input impedance of each pick-up stage should be low enough to allow the collection of such generated photocarriers instead of them contributing to the drain-to-source quiescent current I_{DS0} **18**. On the other hand, however, this input impedance of each measurement channel connected to each measurement terminals M_i **43**$^{(i)}$) should be high enough as not to disturb the drain-to-source potential distribution along the channel **5** (i.e. avoid sinking in/pouring out any important contribution from/to the drain-to-source quiescent current I_{DS0} **18**) and at the same time also to provide a significant (i.e. measurable) voltage drop across it due to the appearance of a photogenerated current $I_{ph\,i}$ **44**$^{(i)}$. Alternatively, one can have all the read-out pick-up circuitry with an extremely high input impedance, and instead of measuring the collected photocurrents $I_{ph\,i}$ **44**$^{(i)}$, one would measure the variation in the voltage drop along the channel (i.e. the change in the potential at each measurement terminals M_i **43**$^{(i)}$) as the drain-to-source current will now be modified due to the additional component **181** determined by the photogenerated components.

Finally, the metal contact **7** corresponding to the top gate contact regions **29** should be realized either as depicted in Fig.36, i.e. of small dimensions within the illuminated area **19** so as to block as little light as possible, or they can be made to extend fully along the entire length of each contact

region **29**. Evidently, in this latter case a transparent metal, like ITO, must be used in order to employ the device as a photodetector.

The previous discussion referring to the A.2.2 spectroscopic colour sensor of Fig.36 started as being just one possible embodiment of a colour sensors realized using the A.2.1 generic structure of Fig.35. Another possibility is to try and use the structure as already briefly mentioned when discussing Fig.35: the opaque regions **42** are arranged such that photogeneration due to various wavelengths of incident light takes place in various regions of the device. However, the most significant disadvantage of the A.2.1 device in Fig.35 for such a colorimetric application is the varying width of the depletion region along the channel region **5**. A possible solution is to have no reverse bias applied on the superficial top region **5**, and even more than that, to clamp its potential at the same value as that of the surrounding epi region **3** in order to have a minimal and constant width w_B **164** of the depletion region **16** along the entire channel region **5**. In such a case, the structure of the device is the one shown in Fig.39-a. The strongly doped regions **6** are now different, as **61** and **62**, each realized to have junctions **461** and **462** of different depths. The drain **11** and the source **8** are now both connected to positive supply biases ($V_D > V_S$) of values required to generate the depletion widths w_g **163** and w_R **165** necessary to allow absorption of the green and red light components **202** and **203**, respectively. Clamping the potential of the entire channel region **5** at the same value as that of the epi region **3** can be done as shown in Fig.39-a, by regularly introducing small diffused regions **42** of the same type as the epi region along the channel **5**, and which are also electrically connected (using Al metallizations **7**) to the channel **5**. Light of different wavelengths (**201, 202, 203**) incident unto the exposed areas of the device will then induce photogeneration of free carrier pairs **22, 50** and **25**. The holes will form substrate currents **451, 452,** and **453** that are all contributing to the total photocurrent **45**. The electrons will determine the appearance of the currents **23, 471** and **26**, which can be sensed either directly or as a variation of the currents unto which they superimpose (the corresponding current meters are not included in Fig.39-a).

However, this solution would introduce even more inconvenient drawbacks. As both drain **11** and the source **8** are now connected to positive potentials and the top gate contact **9** has to be connected to the same potential as the epi region **3** in order to minimize the width of the channel's depleted region, it results that drain-to-gate and source-to-gate quiescent currents **47** and **48** will flow through the device as shown in Fig.39–a. Moreover, given the relatively small dimensions of the device and the high doping levels in the regions **61, 62** and **42**, the intensity of these currents is likely to be quite high, and thus such a device would be uneconomical in usage (high quiescent power consumption). Consequently, other better solutions are proposed here. The first one is shown in Fig.39–b. The structure is very similar to the previous one shown in Fig.39–a. The main difference is that the contacting regions **42** and their corresponding contacts **7** are eliminated and a 'buried' layer **52**, of the same doping type as the epi region **3** but of much higher doping concentration, is now introduced under the channel region **5**. This region **52** can easily be realized practically, using either epitaxy (so that regions **52** and **5** will be grown sequentially, followed by diffusion of regions **61** and **62**) or –simpler- just by implanting the desired dopant in the wafer. This implantation should be optimized so that the average penetration range (R_P) of the implanted ion and the subsequent doping profile peaked at a sufficient depth and decreased rapidly towards the surface, even after a short activation anneal. This would generate the desired 'buried' region **52** while at the same time allow the generation of the shallow channel region **5**.

The effect of introducing the 'buried' region **52** is easy to understand: the doping of this 'buried' region **52** is much more significant than that of the epi region **3**, at least comparable with or higher than that of the channel region **5**. Consequently, only a very narrow depleted region can be formed here, extending only within the channel region **5**. Its width may still be varying from the source towards the drain, but this variation is now negligible as the entire depleted width is no longer significant (as was in Fig.35 due to the free extension into the very low doped epi region **3**) but reduced to extremely low values (e.g. tens of nanometers) due to large doping concentrations of both the channel region **5** and the'buried' region **52**. This means that the spectral selectivity towards the shorter wavelengths of the light component **201** will be determined by the depth of the junction **41'** of the'buried' region **52** with the channel **5**, and by the doping of the channel region **5** (if much lower doped than the 'buried' region **52**).

The shortest wavelengths of the light component **201** (violet and possibly some near ultraviolet light as well)) that is falling in the channel region will therefore be absorbed in the immediate vicinity of the device surface. As such, they would determine photoconductivity modulation **353** within this channel. Furthermore, the slightly longer wavelengths (blue) of the light component **201** will penetrate slightly deeper and induce photogeneration of free carrier pairs **22**. As shown in Fig.39–b, the addition of a top gate terminal **9** connected at a desired potential is now optional. If this terminal **9** exists, then one can detect the 'blue' current component **23** using a current meter (not drawn in Fig.39–b) as a variation of the quiescent current **49**. Of course, in such an arrangement all the quiescent currents would exist, too (in broken lines in Fig.39–b), although at much reduced intensities due to the different structure (extremely narrowed channel region **5** due to the extension of the depleted region in this portion). If this top gate contact **9** is not present, then the photogenerated electrons will form a current **181** that will contribute to the drain-to-source current I_{DS0} **18**. (For simplicity, any necessary current meters were not included in Fig.39-b, but one can assume their presence whenever it is practically necessary to measure a certain current at that respective terminal).

Therefore, a further improved embodiment is proposed here in order to completely eliminate the necessity of using a direct electrical connection to the gate region **5**, while at the same time being capable to detect separately the colour photocurrent generated in the channel region **5**. This version is shown in Fig.39–c, and it consists of the same structure as the device of Fig.39–b, only that a MOS gate is now used instead of the one electrically connected directly to the channel region **5**. The biasing potential **91** applied unto the gate **9** is selected such that the device is in strong depletion mode or -at the most- in weak inversion with only a small subthreshold drain-to-source current I_{DS0} **18** flowing through the device. This means that now the depleted region extends throughout the width of the entire channel region **5**. Therefore, all the wavelengths in the light component **201** incident unto the gate region (it is assumed that the gate metal **71** is transparent and no interference effects appear due to the gate oxide **72**) will induce photogeneration of free carrier pairs **22**. Now, however, unlike the previous case, the electrons will contribute to the channel charge. This can have two detectable effects: first, this supplementary channel charge will require a corresponding modification of the gate potential ΔV_G **93**; secondly, this supplementary channel charge will form a current **181** that will contribute to the drain-to-source current I_{DS0} **18** with an extra component ΔI_{DS} **18'**. Setting the transistor in weak inversion mode is important: first, it minimizes the quiescent current **18** through the device and thus maximizes the read-out of any variation due to photogeneration. Secondly, because in this region I_{DS} decreases rapidly with V_{GS}: at ~0.2V below V_T, the fall becomes exponential, similar to the I_C vs. V_{BE} of a BJT. The subthreshold current in this region has the general form:

$$I_{DS} = I_{DS0} \exp\left(\frac{qV_{GS}}{nkT}\right) \qquad (1)$$

with n>1. In eqn. (1) it can easily be noticed the strong dependence of the drain-to-source current on the gate potential. Hence, any variation in this gate potential (like that required to compensate for the extra charge appeared in the semiconductor due to photogeneration) will lead to an amplified response in the drain-to-source current. In other words, our device operates like a quasi-phototransistor, but with a MOS gate, and the 'base current' leading to significant responses (i.e. detected variations) is actually provided by the photogeneration induced by short wavelengths light component **201**.

Either of the above mentioned responses can be measured and can be used to extract the colour information. Two reference transistors may be necessary: one which is completely opaque to all incident light **20** (not shown in Fig.39–c), and one with only an opaque gate.

Fig.39-d shows some important elements in one possible layout implementation for the stand-alone discrete realization of the A.2.2 device shown in Fig. 39–b. It can be seen that the source & drain metallizations (presumed to be made of opaque Al) are placed only at the edges of the corresponding source & drain regions **61** and **62** in order to expose to light only the interior of these regions. The gate can be realized in more ways: one of them is to have a simple uniform square layout for the channel region **5**. Fig.39-d shows another possibility, in which the channel region **5** is realized as a combined vertical & horizontal lines intersecting each other in a grid-like pattern. This pattern for the channel doped region **5** would therefore be bordered by the depletion region **16** which will not be limited only underneath the doped region **5**, but can now extend vertically, too, up to the wafer surface. This may have an advantageous impact in improving the spectral selectivity for very short wavelengths towards near-ultraviolet, but one may need to be careful to take necessary measures and

ensure a very good quality of the surface to prevent any increased leakage due to recombination-generation effects. An increase in overall gate area may also be necessary, as on the same surface the grid-like pattern will have a smaller active area unto which light can efficiently generate the desired effect in the channel region **5**. Because the channel region **5** may not have a sufficiently high doping level, a strongly doped and very shallow region **53** may need to be added for a good electrical contact between the interconnection metal and the silicon.

This layout can also be used for the discrete MOS device shown in Fig. 39–c after corresponding changes for the gate region which should be made continuous (uniform square) and fully covered with a transparent metal to allow the application of the necessary gate potential. For such a MOS realization, miniaturization of the device and its application in imaging arrays becomes easily possible (although, in principle, it is also feasible for the JFET version of Fig.39-b, too, but without any gate contacts and gate electrodes). Again, a convenient way to structure the array is to use a similar approach like that shown in Fig.s 34-a or 34-c and to merge together the source & drain regions of the transistors situated on neighbouring columns (as in Fig.34-c), or even to merge the sources in a single column, as in Fig.34-a. In either case, however, in order to have an array made of devices based on the A.2.3.c structure, the gate must be of MOS type. The resulting array will consequently be operated with signals very similar to those detailed in Fig.34-b. And as it was mentioned when discussing the arrays of Fig.s 34-a and 43-c, circuitry can be added in each pixel, right next to the colour sensing structure in order to aid the easy matriceal selection of each pixel, to carry out some preliminary amplification of the output signals provided by the pixel sensor, and then to route them towards the signal processing circuitry that will extract the final colour information from these signals.

The last JFET-based type of structure is actually the result of combining together in a single structure both JFET-based colour sensing devices previously devices: with bulk (A.1.1 type) and surface (A.2.3 or A.2.1) channels, respectively. All these A3 type of devices are most suited for multi-wavelength domain detection, i.e. different wavelength ranges will generate various effects at different depths, which will be detected using a multijunction structure and allowing one to obtain more than 3 colour signals.

Fig.40 shows the internal structure of the first example of such a complex device. Its elements and their meaning are discussed and explained as follows (the meaning of the elements not mentioned here remains the same with the similar elements having the same numbering in the previous Figures).

In Fig.40 one can immediately recognize the basic A.1.1 structure, with bottom gate region **1** contacted using a deep strongly doped diffusion **14**, and the source and drain regions **6**. The applied external bias supplies **81**, **101** and **111** make that a quiescent current I_{DS1} **18** is flowing through the channel within the epi region **3**. The top gate region **4** is also present, and the top and bottom depletion regions **15** and **16** form at the junctions **12**, **13** and **17**, respectively. However, the top gate region is now itself used as a 'well' region in which two more JFETs are realized. In the first of them, region **4** itself plays the role of the channel region, and is therefore contacted using two additional strongly doped, but not deep, regions **42**. The applied external bias supplies **91** and **321** make that between these $D_2 \equiv G_1$ and S_2 terminals **9** and **32**, a quiescent current I_{DS2} **37** is flowing. This JFET could also have a uniform top gate region, but one can again use this top gate region for a last JFET (or MOSFET) structure. This second JFET can then be realized by using region **4** as bottom gate, strongly doped regions **29** will form its source and drain, and the gate is realized using either a very shallow (and less doped) region **30** (as shown in Fig.40), or by simply using instead an MOS structure with an additional transparent top gate metal electrode (not shown in Fig.40). The applied external bias supplies **341** and **332** (plus a necessary gate bias, in the case of an MOS gate structure) make that a quiescent current I_{DS3} **39** is flowing through the channel region **30**. It can be noticed that the positive potentials **341** and **91** that act as drain biases for some ('upper') JFETs are also playing the role of gate potentials for ('lower') JFETs underneath the former ones. This effect, combined with the application of the bottom gate biasing **101** for the lowest JFET, results in developing the depleted regions **15**, **16** and **31** which effectively isolate each drain-to-source current path from one another.

The operation of the device is then a straightforward extension of that of the device A.1.1 shown and explained in Fig.32. In that device, the spectral responses were caused by the effects of three light wavelength ranges, R, G and B, respectively, which are absorbed at different depths.

Because of the multi-junction *npnp* structure of the device in Fig.40, one can now obtain responses that are influenced by more and narrower light spectral ranges, and their wavelength limits will be determined by designing appropriately the depth of all the junctions as well as the doping levels of the various device regions. (***Note:*** *due to lack of space in Fig.40, some light-related phenomena and the resulting effects were depicted to take place outside the active/illuminated region* **19**, *although, obviously, in practice this is not the case*). The depleted region **15**, developing around the deepest junction **12**, will still respond only to the longest wavelength range, namely the red (R) part **203** of the incident light. Only in this region the R part of the spectrum photogenerates free carrier pairs **25**, which are instantaneosuly split up and contribute to the bottom gate current I_R **26**, and to the current component **182** that is added to the quiescent drain-to-source current I_{DS1} **18**. The light components with slightly shorter wavelengths, i.e. orange (O) **204**, penetrate to a smaller depth and thus determine photoconductivity modulation **351** of the quiescent drain-to-source current I_{DS1} **18**. The Yellow (Y) component **205** of the incident light has a similar effect in the depleted region **16**, as the red one **203** has in the depleted region **15**: free carrier pairs **36** are photogenerated and split up so as to contribute to the current component **371** that is added to the quiescent drain-to-source current I_{DS2} **37**, and to the current component **181** that is added to the quiescent drain-to-source current I_{DS1} **18**, respectively. The G (green) component **202** can penetrate only up to the depth corresponding to the channel of the second JFET (i.e. the one realized in the gate region of the bottom-most JFET), where it is absorbed and determine photoconductivity modulation **352** of the quiescent drain-to-source current I_{DS2} **37**. The B component **201** of the incident light has an effect in the depleted region **31** (developed at the junction **41**) similar to those determined by the Y component **205** in the depleted region **16** and by the red component **203** in the depleted region **15**, respectively: free carrier pairs **22** are photogenerated and split up so as to contribute to the current component **372** that is added to the quiescent drain-to-source current I_{DS2} **37**, and to the current component **401** that is added to the quiescent drain-to-source current I_{DS3} **40**, respectively. Finally, the light component **206** with the shortest wavelengths (violet), is immediately absorbed at the very surface of the wafer or in its immediate proximity, so as to determine photoconductivity modulation **353** of the quiescent drain-to-source current I_{DS3} **40**. In conclusion, the following total influences occur:

- The final drain-to-source current **54** of the first (bottom-most) JFET structure is resulted from the O-induced photoconductivity modulation **351** of the quiescent drain-to-source current I_{DS1} **18**, and the addition of the supplementary R- and O-originated currents **181** and **182**, respectively;
- The final drain-to-source current **38** of the second (middle) JFET structure is resulted from the G-induced photoconductivity modulation **352** of the quiescent drain-to-source current I_{DS2} **37**, and the addition of the supplementary Y- and B-originated currents **371** and **372**, respectively;
- The final drain-to-source current **40** of the third (top-most) JFET/MOSFET structure is resulted from the V-induced photoconductivity modulation **353** of the quiescent drain-to-source current I_{DS3} **39**, and the addition of the supplementary B-originated current **401**, respectively.

Consequently, in this case much more complex signal processing has to be carried out in two steps in order to separate the final desired chromatic information: first, the spectral output is separated by subtracting the similar signals from a reference device, and also using both the drain and source current meters' indications for the same device but in a differential manner. Secondly, once the colour signals are obtained from the raw outputs provided by the device, they may need to be again processed in order to obtain the desired final spectral data.

The device shown in Fig.41-a is functionally similar to the one presented in Fig.40 as it is made up again of three vertically stacked JFET transistors, realized by growing three subsequent epitaxial regions regions **3**, **300** and **301** of rapidly decreasing thicknesses (e.g. of 10...20, 2...4 and 0.05...0.2 μm, respectively) that are separated by patterned buried layers of opposite doping type **27** and **271**, respectively. The doping concentrations of the epitaxial regions are also very similar to those of the regions used in the devices discussed previously and presented in Fig.32 or Fig.40. For instance, the p^- epi region **3** can have a doping level in the range $10^{14}...10^{16}$ cm^{-3} (the low value would demand a large thickness, and viceversa), the middle p epi layer **300** can have a doping level in the range $10^{16}...10^{17}$ cm^{-3}, and the top $p+$ epi layer **301** can have a doping level in the range $10^{17}...10^{18}$ cm^{-3}. The top-most $n+$ region 30 should be extremely shallow (e.g. 0.05...0.1 μm), with a surface doping

level in the range $10^{18}...10^{19}$ cm^{-3}. In fact, its presence is optional, and in case it is chosen to be included in the structure of the device its parameter values (doping and thickness) would determined the short-wavelength responsivity of the device.

After growing the epi layers, S & D strongly doped regions of increasing depth **42**, **421**, and **422** are then diffused in order to allow contacting the device and minimizing the overall channel resistance. However, the main difference compared to the previous case is that the top gate region of an underlying JFET is not confounded with the drain region of its upper neighbour. Instead, gate strongly doped regions separate each JFET from one another. These regions are obtained by first carrying out a patterned diffusion of the buried layers **27** and **271**, which will be contacted with the strongly doped regions **143** and **145**. This will effectively define the channel regions using the epi regions **3**, **300** and **301**, respectively, in separate "tubs" that encircle one another. The strongly doped substrate **1** is contacted using a strongly doped region **142** diffused after the etching of deep trench in which a dopant source (e.g. strongly *in-situ* doped polySi) was deposited after a brief oxidation, underwent a drive-in anneal, filled in (also with polySi) and then planarized using Chemo-Mechanical Polishing (CMP). The same technique will be exploited later, too, for the FCT-based device that will be presented in Fig.44. In fact, it is feasible that even all the deep diffused regions **42**, **421**, **422**, **142**, **143**, **145** could be realized using such techniques, applied in sequence, with trenches of corresponding depths and using the correct dopant type. One advantage is that the subsequent application of such trench-based diffusion methods minimizes the thermal budget, as compared to the typical oven-based diffusions. Even if the drive-in anneal steps would be executed using Rapid Thermal Annealing (RTA) tools, the lateral diffusion of the dopant would still remain comparable to that of its depth of diffusion. Therefore, this method also allows a better area usage on the chip. This is especially important as this device tends to be quite large, due to two facts: first, the large number of terminals due to the existence of separate terminals and contact regions for each and every transistor; secondly, because the strongly doped contact regions **42**, **421**, and **422** used for the drains should be distanced from the gate region, as these regions exhibit maximal extensions of the depleted regions, which develop starting from both the gate region and the drain region into the channel. This means that area saving can be done only if the D terminals are specifically identified and used as such (the S regions can be situated closer to the gate regions); if S & D contact regions are implied to be interchangeably used according to the momentary need, then all the contacting regions **42**, **421**, and **422** must be maximally spaced with respect to the gate contacting regions **142**, **143**, and **145**, and any common interconnection of all the S regions should be eliminated from the layout. Fig.41-b schematically shows a possible layout realization, in which the S & D regions are each specifically identified as such. This can be seen also from the larger separation between the D and the G contacting regions (as compared to that between the S & G regions, respectively), as well as from the common shorting of all the sources together, as they would all be connected to the GND. It must underlined that the drawing did not include the mask for opening of contact windows in oxide or any other protective insulating layers that may be deposited on the devices. For convenience, these insulating layers were omitted from Fig.41-a, as from any cross-sectional drawing presented in this paper. Regions **42'**, **421'**, and **422'** are optional, but can be included if the user wants to prevent the depleted regions to extend laterally from the vertical gate contact regions, thus allowing the control upon the channel region to originate only from the depleted regions that are developed by the horizontal buried layer regions (their masks are represented by broken lines in Fig.41-b). The mask defining the active exposed window **19** is also not represented, but it is has dimensions and location comparable to that of the topmost region **30**, which is also optional as it actually can be removed. As mentioned above, its presence, or –if it is included- its parameters (depth & doping) may be chosen depending on which specific wavelength range of interest is desired to impact a certain region or another of the upper-most JFET transistor (to be absorbed, to photogenerate free carriers in a depleted region or to modulate the conductivity in the channel using the epi region **301**).

More specifically, one can design the thickness of each epi region depending on which wavelengths of interest are to photogenerate free carriers in the depleted regions (which will extend both upwards and downwards from the gate buried regions **27** and **271**) and which will photomodulate the conductivity in the channels using the epi regions. This can be easily understood by extending the functioning for the device presented in Fig.40, for this device shown in Fig.41-b. One can thus design appropriately the device so that the red, green and blue wavelength ranges of the visible spectrum will

photomodulate the conductivity in the channels, and use only these as the most important output signals, discarding the other ones.

Fig.42 presents various versions of the previous device, each with alterations or modifications compared to the original sketch of Fig.41-a. This, the version in Fig.42-a shows the same device, but in which each transistor is clearly delineated by performing an extra dry etching step. This is another alternative, which does not require trench etching and filling. Nevertheless, it still requires dry etching to define the silicon islands in which each device is situated, and then –optionally- thick oxide deposition followed by planarization (not shown in Fig.42-a). The advantage in this case is that only one mask would be used to define all the S & D regions **42**, **421**, and **422** (and **42'**, **421'**, and **422'**, if desired to include them), and also a single mask for all the G contact regions **142**, **143**, and **145**. As only one short diffusion step is now used to define each of these S, G & D contact regions, they will all have the same appearance as regions **42** and **145** in the first device shown in Fig.41-a. This would greatly reduce the complexity and thermal budget of the entire processing, and also reduce drastically the number of necessary masks. Moreover, in certain situations the thick oxide deposition and subsequent CMP planarization steps may not even be necessary. This is because for certain wavelength ranges, and certain applied drain bias values, thin epitaxial regions **300** and **301** may be used, so that the maximal step size of the relief on the wafer surface could be around 1...2 μm. Under these circumstances, it could be possible that direct alignment can be done in the photolithographic steps even in the presence of such releief steps, depending on the type of machine used, the thickness of photoresist employed and the resolution of the process. Non-demanding processes, e.g. with a 2-μm resolution, may accommodate such photolithography directly on the etched relief surface of the device.

Fig.42-b shows another simplification that can be brought: all the transistors would have a single common source region. This would reduce significantly the layout area for the device, as it can be noted from Fig.42-c which shows a possible layout representation of this device version. However, the main drawback of this device is that user would have to tolerate the existence of 'cross-talk' between the channels of the different transistors. Because the horizontal strongly doped gate regions **30**, **271** and **27** have to be situated at some minimal distance d_{min} from the source region **422** (its value being dictated by the extension of the depleted regions into the low doped epi regions), there could still exist –even after developing the depleted regions- the possibility for a current flow route between two different drains of neighbouring JFETs due to the potential difference between their drain bias voltages. Nevertheless, the influence of this factor could be very small because of the very large resistance for this current flow path. This is due to both the large length (two channels in series), as well as the resistance of the 'neck' region between the doped gate regions **30**, **271** and **27** and the source region **422**, which is much narrower than the physical distance d_{min} (it was narrowed down because of the development of the depleted regions). Moreover, the problem can be easily alleviated if one uses the device not by simultaneously biasing all the drain terminals at the same time, but sequentially. And of course, although not depicted, one may combine the etch delineation method of the previous Fig.42-a device for such a common source device, too, resulting in a further simplification, making the common source device highly suitable for usage as a pixel in imaging arrays.

Lastly, the most compact realization of the A3 JFET-based colour sensing devices can be achieved by using not only a common source, but also a common gate for all the transistors. Fig.s 43-a and –b show the layout of such a device, and its structure, respectively. It can be seen that, indeed, it can be reduced to the smallest possible size. Fig.43-b shows the cross-sectional view along the B-B' line. It can be seen that the device still consists of three vertically stacked 'decks'. Having a unique gate region means that the device is most suited for applications in which the colour info provided by the gate signal is not essential, and if necessary can even be discarded. In this case, the device is intended to be designed such that the red, green and blue wavelength ranges of the visible spectrum would photomodulate the conductivity in the channel regions in the middle of the depleted regions, as shown in Fig.43-b. The common source structure also calls for a sequential biasing of each drain terminal, but this can be easily done in an array realization in which each pixel anyway is addressed sequentially. As already highlighted in Fig.42, the cross-sectional view along the A-A' will result in exactly the same drawing as that shown in Fig.42-b. Again, further simplification of the device can be

achieved if one combines the common-gate and –common-source approach with the etch delineation one.

The final type of devices to be presented are the FCT-based ones. As it was detailed in the previous sections describing the previously existing art, the structure is derived from that of an FCT/SIT power device. Fig.40-a shows the structure of the proposed device. It consists of a highly doped $n+$ substrate **1**, on which an epitaxial region **3** of the same type of doping was grown. The substrate itself plays the role of the cathode (K) of the entire device, whereas the epi region is necessary to realize in it the anode (A) and gate (G) regions **4** and **14**, respectively. These regions are of opposite doping ($p+$) in comparison with that of the substrate **1** and the epi region **3**, and have high doping concentration. Their realization within the low doping concentration epi region **3** ensures that any depleted region will extend almost completely only within the epi region **3**. The anode's $p+$ doped region **4** is much shallower than the two lateral $p+$ doped region **14** of the gate. As it can be seen in Fig.44-a, these two gate regions are extended much more in the x direction, i.e. oriented much more in depth than the lateral extension along the y axis, i.e. along the surface of the device. Moreover, in a real device, the $p+$ regions **14** which appear represented in Fig.44-a as two separate elements, may in fact belong to a single ring-like, or surrounding, $p+$ gate region that completely circumscribes the central anode's $p+$ doped region **4**.

It is clear that between the A & K contacts **55** and **60**, respectively, the device is basically a $p+nn+$ diode, placed between the gate $p+$ regions **14**. In the typical power applications, a forward bias is applied between the A & K contacts **55** and **60**, and the device can be switched OFF when a strongly enough negative gate potential is applied unto the gate terminal **9**. Alternatively, in order to achieve a device that is normally OFF, the doping of the n epi region **3** is made low enough, and the spacing between the gate regions small enough (sometimes in a buried arrangement under the anode region itself) so as the depleted regions **15** developed at the $p+n$ junctions **17** around the gate $p+$ regions **14** would touch each other and completely seal off any current channel even without an applied gate potential. In this case, however, unlike the power device operation, the A junction **13** is not forward, but also reversed biased using an external bias supply **551** through a high resistance value resistor **553**. Similarly, the reverse bias unto the G terminal **9** is applied using an external bias supply **91** through a high resistance value resistor **93**. Under these circumstances, the functioning of the device is as follows.

Asuming there is no applied anode bias, depleted regions **15** develop at the $p+n$ junctions **17** around the G $p+$ regions **14**, and they will extend laterally towards the A within the interior region of the G ring. The extent of this lateral extension is dependent on the value of the applied reverse gate bias **91** and the doping value of the low doped epi region **3**. Likewise, if an anode reverse bias **551** is applied on the A terminal **55**, the anodic depleted region **16** will attempt to extend laterally as well as in depth, following the contour of the junction **13**, with an extension value dependent on the voltage of the applied reverse A bias **551** and the doping value of the low doped epi region **3**. This extension will isotropically continue both laterally and in depth, always reproducing omothetically the topological contour of the junction **13**, but enlarged with a quantity which can be calculated according to the well-known formula of dependence between the width of a depleted region and the applied voltage:

$$w \approx \sqrt{\frac{2\varepsilon_r \varepsilon_0}{qN_{Bulk}} \cdot \Phi_{Tot}} \qquad (2)$$

where N_{bulk}= the doping of the low doped substrate (here, the n epi region 3), ε_r= silicon's relative permittivity (=11.7), ε_0= vacuum's permittivity (=8.856 × 10^{-14} F/m), and Φ_{Tot}= the total potential across the junction=V_R+ Φ_{bi}, with Φ_{bi}= the junction's built-in voltage, given by:

$$\Phi_{bi} = \frac{kT}{q} \ln \frac{N_A N_D}{n_i^2} \qquad (3)$$

in which n_i= intrinsic silicon concentration of carriers= 1.45 × 10^{10} cm^{-3} and $N_{A,D}$= the doping concentrations of the p and n regions, respectively.

However, if the G $p+$ regions **14** are also reverse biased, the extension of the A depleted region cannot continue unhindered. Some of the area between the G $p+$ regions **14** has already been occppied by the depleted region **15** developed by the gate. As this area next to the gate regions has already been depleted, the anodic depleted region **16** has no other choice but to extend in depth, downwards, as it

can expand only along that direction in order to evacuate the necessary free carriers as imposed by the externally applied bias supply **551** (as long as the anodic and gate biasing potentials **551** and **91**, respectively, obey the relation $V_A<V_G$). The external resistors **93** and **553** serve as current limiting components once the two depleted regions meet each other.

As a result, for a given gate potential, the anodic depleted region **16** has no other choice but to extend much faster in depth after it has encountered the lateral G-induced depleted regions **15**. Therefore, the depth of the anodic depleted region **16** is now a function of both V_A and V_G: for a constant V_A, varying V_G should determine a deeper or shallower extent of this depleted region **16**. Similarly, for a constant V_G, varying V_A should determine a deeper or shallower extent of the depleted region **16**, as shown in Fig.40-a by the two depths **56'** and **56''** obtained for two different anodic reverse biasing voltages $|V_{A2}|>|V_{A1}|$. It must be highlighted that these two depths **56'** and **56''** are obtained for much lower applied reverse bias values than those theoretically predicted by eqn. (2). Reversely, at the same applied reverse bias values, the anodic depleted region **16** will exhibit much wider depths than those theoretically predicted by eqn. (2).

Consequently, the main advantage of the device becomes now clear. One can easily modulate *electrically* the diode's spectral response (i.e. that of the anodic current measured with the current meter **552**) using the separate G control voltage: for different gate voltage values different depths for the depleted region **16** result, hence the anodic spectral curve will become more shifted towards the red part of the visible light. This allows for potential area saving in terms of "chip real estate" in colour-sensitive devices, as it eliminates the need for large arrays with numerous fixed-in-place identical detectors but each having different filters on top of the silicon. Furthermore, this solution is also ideal for increased design flexibility as allows immediate interfacing with signal processing circuitry and feedback control logic.

The exact initial shape of the anodic spectral response, as well as the modified ones obtained under different applied G voltages, also depend on the extent of the active area **19** (the rest of the device is considered as shielded against light with an opaque, typically metallic, mask layer). For most accurate results this area **19** should be situated only within the limits of the A $p+$ region **4**. Moreover, in order to photogenerate a large response signal the anodic area should be large, i.e. the lateral anodic distance l_A **57** should be large. However, the requirement to easily influence the depth extension of the anodic depleted region **16** asks for a rather small value of l_A **57**, so that the two G $p+$ regions **14** would be as close as possible to one another, which means that a short anodic length l_A is requested. Besides these two contradicting requirements which need to be compromised, another factor appears, too: if the extent of the active area **19** is as shown in Fig.40-a, the device's spectral response will depend on two parts of the anodic depleted region. The first part extends in depth, under the anode's $p+$ doped region **4**, whereas the second part comprises the lateral extensions, from the surface of the device and into the bulk down to the final extension depth. For certain A & G potential values it is also possible that even some part of the gate depleted region **15** may also be included within the illuminated area **19**. All these components will therefore modify accordingly the spectral response, so the designer has to initially consider all the necessary factors and find the necessary solution for the extent of the illuminated area **19** that is most suitable for his needs.

However, because the device presented in Fig.44-a is based unto the classical structure of a FCT power device, it was tacitly assumed that the G $p+$ regions **14** are realized as in an FCT, namely by trench etching into the in the epi layer **3**, followed by epitaxial fill-up with strongly doped $p+$ monocrystalline Si. This technique may be difficult to implement as it requires special know-how and equipment. For this reason, a much more technologically advantageous embodiment of the device is shown in Fig.44-b. Here it can be clearly seen that the G $p+$ regions **14** are realized in a different m,anner: although the first step still remains trench etching into the Si substrate (e.g. through a thick oxide mask, or a oxide-nitride combined mask, with window openings only in the G $p+$ regions **14**), the next steps are different. After etching the trench in the substrate, a deposition of an *in-situ* $p+$-doped polysilicon layer **141** is carried out until the trench is filled completely. This is followed by a short drive-in step necessary to realize the G junction **17** by diffusing the $p+$ dopant in the epi layer **3** and thus realizing the thin $p+$ regions **14'** that follow the contour of the trench. Finally, the polysilicon **141** is planarized using Chemo-Mechanical Polishing (CMP) and then the remaining steps of the process are carried out.

It must be emphasized that this method is much simpler and more convenient to implement in fabrication than performing a long diffusion to reach and contact a region situated at relatively large depth (up to 10 microns). The trench methods minimizes tha area occupied and the latral dopant diffusion, both of which would result in an increased device density on the chip. Consequently, the method can be applied instead of such contacting by deep diffusion in any of the previous devices, e.g. instead of the deep $p+$ contact diffusion **14** for the bottom gate, in Fig.s 32-34 and 40, as well as instead of the deep drain region **62** in Fig.s39-a, b, and c.

Another major difference from Fig.44-a, is that Fig.44-b also highlights the read-out method implemented using a circuit that plays the role of the previous current meter **552**. It can be seen in Fig.44-b that the resistor R_A **553** has two functions: first, as presented in Fig.44-a, it's high value of should limit (together with R_G **93**) the current that may appear when the anodic and gate depleted regions, **16** and **15**. Secondly, using the high-impedance differential amplifier A_1 **554** one can also detect the variation in the reverse anodic current that appears due to photogeneration by reading the voltage drop that appears across this resistor. The "dark current" value, read from an identical 'blind' reference (i.e. not-exposed to light) device and read through an identical amplifier A_1' **554'** (not shown in Fig.44-b) can subsequently be subtracted from this value using a second high-impedance differential amplifier A_2 **555** which finally provides the desired output signal **555**. This means that resistor R_G **93** can have any high enough value (e.g. ~MΩ, or bigger) considered suitable for current limiting purposes, whereas the resistor R_A **553** should have a value scaled such that it would provide a desired voltage drop across it under certain light excitation conditions. Of course, another possibility would be to use only a single amplifier A_1 **554**, and instead of employing a separate identical 'blind' reference device, to carry out the readings in two stages; first under darkness (calibration), and then under illumination. However, this latter possibility may not always be advantageous, as it requires light chopping using mechanical, or other types of, methods. This would increase the volume of the final system and also make it heavier and more expensive and prone to failures.

Finally, if so desired, the gate regions may also be exposed to light and the gate current variations due to photogeneration monitored in a similar manner as for the anodic ones (i.e. implementing a similar read-out circuit that would play the role of the current meter **92**).

Fig.44-c shows the same device, but in a simplified version. It can be seen that both the $p+$ regions, the top anodic one **4** and the lateral gate one **14'**, are now merged in a single continuous $p+$ region **144** of varied depth profile. In this case the principle remains the same: the lateral expansion of the A&G depleted region **156** will logically be smaller (**156'**) for lower values of the applied external bias V_{AG} **5591**, and will increase (**156''**) for larger reverse bias values. However, just as in the previous cases, under the junction **13** of the superficial $p+$ region (the ex-anodic region), the depleted area has to extend not only laterally, but also downwards. Therefore, the lateral development encouraged by the deeper gate junctions **17** will force the downward extension of the horizontal depleted region to a deeper or shallower extent, as shown in Fig.44-c by the two depths **56'** and **56''** obtained for two different anodic reverse biasing voltages $|V_{AG2}|>|V_{AG1}|$. It can be seen that the difference between these two depths **56'** and **56''** is much wider than the difference between the simple lateral extensions **156'** and **156''**, respectively. This is because the same area has to be depleted under the junction **13** in order to achieve final charge equilibrium, but its dimensions will be different because lateral parts have already been depleted by the lateral regions, so the only left alternative is to expand downwards.

The advantage of this device is that no current limiting problems appear. However, in this case there is no decoupling between the spectral control voltage and the read out circuit as they both are now merged into one.

Fig.44-d shows the conceptual structure of an imaging array composed of more identical elements of the B.1.1 type. The only difference is that now the cathodic $n+$ region **1** of the substrate is contacted from the surface of the wafer by means of a deep $n+$ diffusion **100**. Of course, this deep diffusion can also be replaced by a more convenient trench-based lateral diffusion followed by polysilicon trench filling (of course, this trench will have a different depth and a different dopant will be used in this case, than those corresponding to the filled trenches **141** for the vertical gate regions). This technique, as previously presented, can be used to replace any deep diffusion presented in any of

the previous Fig.s, e.g. of regions **14, 62, 146, 143** and **422**, and even for diffusions of reduced depth, like **6, 144**, and **42**, obviously using the necessary depth and corresponding type of dopant as required in each case.

2.4.6- Claims

It should be understood that various alternatives of the embodiments of the invention described herein may be employed in practicing the invention. It is intended that the following claims define the scope of the invention and that methods and structures within the scope of these claims and their equivalents be covered thereby.

What is claimed is:

1. Detectors, mainly based on a junction field-effect operation, (i.e. using JFET-, SIT- or FCT-based structures), intended for usage as
   a) colour sensors that, depending on their specific structure, can simultaneously detect red, green and blue components of the visible light and the same detector comprising bulk and/or surface effects and structures (either single or multiple such structures, alone or combined together as bulk and superficial structures monolithically stacked one unto another vertically, or spread horizontally, in accordance with the intended usage and application of the device), using not only photogeneration in reverse biased junctions but also photoconductivity effects in conductive channels, **or**
   b) imaging devices with superficial-based structures that allow a spectrometric examination of incoming light by detecting various wavelengths in different locations with simultanous outputs provided from those locations at collection/output electrode, **or** that can achieve colorimetric detection by combining the JFET concept with a MOS structure, **or** that can allow a user-controlled spectral response in a FCT- or SIT-based structure,

   each of these detectors being usable either as stand-alone device or as elementary pixel in imaging arrays comprised of a multitude of such elementary colour detectors, and realized in various versions and variants of structures.

2. Detectors, mainly based on a junction field-effect operation, (i.e. using JFET-, SIT- or FCT-based structures), intended for usage as colour sensors that, depending on their specific structure, can simultaneously detect red, green and blue components of the visible light simultanesously, within the volume of one and the same detector comprising bulk and/or surface effects and structures (either single or multiple such structures, alone or combined together as bulk + superficial structures monolithically stacked one unto another vertically, or spread horizontally, in accordance with the intended usage and application of the device), using not only photogeneration in reverse biased junctions but also photoconductivity effects in conductive channels, **or** can be imaging devices with superficial-based structures that allow a spectrometric examination of incoming light by detecting various wavelengths in different locations with simultanous outputs provided from those locations at collection/output electrode, **or** can achieve colorimetric detection by combining the JFET concept with a MOS structure, **or** that can allow a user-controlled spectral response in a FCT- or SIT-based structure, each of these being usable either as stand-alone device or as elementary pixel in imaging arrays comprised of a multitude of such elementary colour detectors, and realized in various versions and variants of structures, as detailed for each of them in the following claims below:
3. A colour photosensing detector with a JFET structure formed in a silicon substrate of a first conductivity type of low or very low doping concentration, for discriminating different light wavelengths in the same location using both photogeneration and photoconductivity modulation, the detailed structure of the colour photosensor comprising:

   a first doped region of a second conductivity type opposite the first conductivity type and of low or moderate doping concentration, preferably formed by epitaxial growth unto the said substrate, the junction between this regions and the substrate being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a first wavelength range of the visible light, i.e. light at the orange-red (longest wavelengths) end of visible spectrum becomes absorbed in the photodiode thus formed, and in which the bottom part of the junction realized in the substrate is identified as 'bottom gate';

a second doped region (denominated as 'top gate') of the first conductivity type and of high doping concentration that is formed in the first doped region, the junction between them being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region (i.e. in the photodiode thus formed) of a third wavelength range in the visible light, i.e. the violet-blue (shortest wavelengths) end of visible spectrum;

a middle conductive channel formed in the **bulk** of the silicon in the first doped region between the said second doped region and the substrate, so that current can pass along this channel between two strongly doped contact regions of the same conductivity type as the first doped region (denominated as 'source' and 'drain', respectively), and whose conductivity is controlled both by the extent of the depleted regions formed at the two said junctions and by the photoconductivity modulation due to carrier photogeneration induced by light absorbed within of this channel which is situated at a depth and has such an extent/width so that these junction depth & depleted width values enable the absorption of a second wavelength range of the visible light within the said channel, light typically in the green-yellow part (middle-range wavelengths) of the visible spectrum, preferably with the absorption peak around 550...555 nm if it is desired to achieve a spectral absorption similar to the photopic response of the human eye;

an opaque region placed on top of the chip such that it allows the exposure to the incident light only of the photosensitive region of interest, namely the central part of the 'top gate' and all the corresponding bulk regions underneath it, respectively;

the photocurrent sensors, or their equivalent electronic circuits, connected to each terminal in order to measure the photocurrents generated by the first and third wavelength ranges of the visible light in the said photodiodes, as well as the current values in and out of the channel so as to detect the variation due to photoconductivity modulation in the middle bulk channel region generated by the absorption of light of the second wavelength range in the said channel, respectively.

4. A colour photosensing detector with a JFET structure as in claim **2**, but with the difference that the bottom part of the silicon substrate is contacted from the front of the wafer using a deep and strongly doped diffusion of the same first conductivity type as the substrate.

5. A colour photosensing detector with a JFET structure similar to that of claim **3**, but wherein a strongly doped buried layer of the second conductivity type opposite to the first conductivity type of the substrate is introduced at the bottom of the channel, in a region located in the same place but slightly more extended in both directions than the 'top gate', i.e. the second doped region of the first conductivity type.

6. An active pixel imaging array, comprising:

(a) a matrix of rows and columns of colour photosensing detectors with a JFET structure, formed in a silicon substrate of a first conductivity type, for discriminating different light wavelengths in the same location, with each colour sensing pixel being a JFET photodetector as in claim **3** with the only difference that the substrate for this array realization needs to be of a high doping concentration, and with the elementary pixel units arranged such that the array structure is as follows:

(i) The 'top gate' regions, realized with the second doped region of the first conductivity type formed in the first doped region, are separately and individually addressable for each pixel;

(ii) The 'drains', i.e. the strongly doped contact regions of the same conductivity type as the first doped region unto which positive external biasing needs to be applied, are merged into a single region common for each two adjacent pixels neighbouring one another along any same row of the array;

(iii) The 'sources', i.e. the strongly doped contact regions of the same conductivity type as the first doped region unto which a zero (i.e. GND) external biasing needs to be applied, are merged into a single region common not only for each two adjacent pixels neighbouring one another along any same row of the array, but also are realized as a single GND

connecting line that extends continuously along an entire column of the array; and

(iv) The 'bottom gate' contact regions, realized with a deep and strongly doped diffusion of the same first conductivity type as the substrate, can be in the shape of a single line common for either all the pixels along an entire row and then repeated next to each row, or for all the pixels in sections of the array comprising more rows and therefore repeated only a few times within the array, or for the entirety of the array, as considered most convenient by the user for the desired performance and specific application

(b) for each pixel in the said matrix, row and column select circuitry for selectively designating the correct order of both applying the necessary external bias potentials and reading or collecting and/or amplifying and processing the output signals representative of the colour information provided by the 'top gate', middle bulk channel, and 'bottom gate' regions, respectively, as was presented in detail in Fig.34-b, either with some circuitry placed in the pixel itself (next to the sensor but not exposed to incident light) and/or with the rest (or the whole) of the signal processing circuitry placed on the same chip but in another area of the device next to the array;

(c) multiple opaque regions placed such that their location and extension allows the exposure to the incident light only for the photosensitive regions of interest and corresponding bulk regions underneath them, namely the central parts of the 'top gate' regions of each pixel, respectively;.

7. An active pixel imaging array, comprising:

(a) a matrix of rows and columns of colour photosensing detectors with a JFET structure, formed in a silicon substrate of a first conductivity type, for discriminating different light wavelengths in the same location, with each colour sensing pixel being a JFET photodetector as in claim 3 but arranged such that the array structure is as follows:

(i) The 'top gate' regions, realized with the second doped region of the first conductivity type formed in the first doped region, are separately and individually addressable for each pixel;

(ii) The 'sources' and 'drains' regions, i.e. the strongly doped contact regions of the same conductivity type as the first doped region, are merged into a single region common for each two adjacent pixels neighbouring one another along any same row of the array, so that the external biasing which needs to be applied is either positive or zero (i.e. GND), depending on how that specific region has to act as a 'source' or as a 'drain' for one or another of the neighbouring pixel along that specific row;

(iii) The 'bottom gate' contact regions, realized with a deep and strongly doped diffusion of the same first conductivity type as the substrate isolated from the rest of the chip using Silicon Trench Insulation (STI), can be either in the shape of a independent and separately accessible contact regions for each pixel, or as a single line common for either all the pixels along an entire row and then repeated next to each row, or for all the pixels in sections of the array comprising more rows and therefore repeated only a few times within the array, or for the entirety of the array, as considered most convenient by the user for the desired performance and specific application;

(b) for each pixel in the said matrix, row and column select circuitry for selectively designating the correct order of both applying the necessary external bias potentials and reading or collecting the output signals representative of the colour information provided by the 'top gate', middle bulk channel, and 'bottom gate' regions, respectively, somewhat similar to that shown in Fig.34-b, either with some circuitry placed in the pixel itself (next to the sensor but not exposed to incident light) and/or with the rest (or the whole) of the signal processing circuitry placed on the same chip but in another area of the device next to the array;

(c) multiple opaque regions placed such that their location and extension allows the exposure to the incident light only for the photosensitive regions of interest and the corresponding bulk regions underneath them, namely the central parts of the 'top gate' regions of each pixel, respectively.

8. A colour photosensor with a JFET structure formed in a silicon substrate of a first conductivity type and of high doping concentration, for spectrometric-like discrimination of different light wavelengths in different locations along a **surface** channel of the same device, the detailed structure of the colour photosensor comprising:

a first doped region of the same first conductivity type as the substrate but of much lower doping concentration, preferably formed by epitaxial growth unto the said substrate;

a second doped region of a second conductivity type opposite the first conductivity type of the first doped region, and of moderately high doping concentration, that forms a superficial channel at the surface of the device, of such a length, with the shallow junction between this region and the said first doped region of the same first conductivity type as the substrate being formed at such a depth, and reverse biased to generate a depletion region gradually increasing in a linear manner from very small to very large widths, so that all these parameter values (length, junction depth & minimal to maximal depleted width) enable the absorption of all the wavelengths in the visible light within the said depleted region, but with different spectral ranges being absorbed selectively and specifically, depending on the exact width of the depleted region in that exact location;

two strongly doped regions also of a second conductivity type opposite the first conductivity type of the first doped region, but of very high doping concentration, located at the ends of the said superficial channel at the surface of the device, that act as as 'source' and 'drain', respectively, i.e. unto which positive and zero (i.e. GND) external biasing need to be applied, respectively, the magnitude of the drain positive biasing determining the *slope* of the depleted region variation along the channel from source to drain, whereas by varying the value of the external bias voltage applied unto the substrate bottom gate region one can control the overall width of the depleted region along the entire surface channel region;

multiple measurement terminals $\mathbf{M}_i$ (i=1...N) equally placed along the superficial channel, implemented using very narrow and extremely shallow and strongly doped regions of the same of a second conductivity type as the channel, with their width and pitch distance dictated both by the desired wavelength resolution to be achieved and the ultimate photopatterning resolution minimally achievable in the actual fabrication;

a multiple read-out pick-up circuitry for measuring either the photocurrents $\mathbf{I}_{ph}$ collected by each measurement terminal $\mathbf{M}_i$, or the variation in the voltage drop along the channel (i.e. the change in the potential at each measurement terminal $\mathbf{M}_i$ as the drain-to-source current will now be modified due to the additional current components that appear within the channel as a direct consequence of photogeneration of carries in the depleted region and their transport in the superficial channel and the substrate region, respectively);

the photocurrent sensor, or its equivalent electronic circuit, connected to measure the total photocurrent collected in the substrate bottom gate region.

9. A colour photosensor, having a JFET structure with a **surface** channel, formed in a silicon substrate of a first conductivity type and of high doping concentration, for colorimetric RGB-like discrimination of different light wavelengths in different locations of the same device, the colour photosensor structure comprising:

a first doped region of the same first conductivity type as the substrate but of much lower doping concentration, preferably formed by epitaxial growth unto the said substrate which can be identified as a 'bottom gate' contact region;

a second doped region of a second conductivity type opposite the first conductivity type of the first doped region, and of moderately high doping concentration, that forms a superficial channel at the surface of the device, which can be identified as 'top gate' and which –if so desired– can be contacted with a separate terminal;

a third doped region of the same first conductivity type as the first doped region but of very high doping concentration, underlying the said superficial channel region on most of its length (except for some safety margins at both channel ends), the junction between this

region and the said superficial channel region being formed at such a depth, and reverse biased to generate a depletion region of such a width extending either across almost the whole channel region, or completely depleting it in its entirety, so that these junction depth & depletion width values enable the absorption within the said depleted region of a third wavelength range in the visible light, i.e. the violet-blue (shortest wavelengths) end of visible spectrum;

a 'source' realized as a strongly doped region also of a second conductivity type opposite the first conductivity type of the first doped region, and of moderate depth penetration in the said first doped region, the junction between this region and the substrate being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption of a second wavelength range in the visible light, i.e. the green-yellow part (middle-range wavelengths) of the visible spectrum, preferably with the absorption peak around 550...555 nm if it is desired to achieve a spectral absorption similar to the photopic response of the human eye;

a 'drain' realized as a strongly doped region also of a second conductivity type opposite the first conductivity type of the first doped region, and of very large depth penetration in the said first doped region, the junction between this region and the substrate being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption of a first wavelength range in the visible light within the said depleted region, i.e. absorption of the orange-red (longest wavelengths) end of visible spectrum in the photodiode thus formed with the said first doped region contacted by the 'bottom gate' substrate region;

multiple opaque regions placed such that their location and extension allows the exposure to the incident light of the photosensitive regions of interest and the corresponding bulk regions underneath them, namely the central parts of the 'source', 'drain' and 'top gate', respectively;

the photocurrent sensors, or their equivalent electronic circuits, connected to measure either directly the photocurrents flowing through a specific terminal, or the variation compared to the quiescent state that may appear due to, e.g., photoconductivity modulation generated by the absorption of light of the second wavelength range in the said superficial channel region, respectively.

10. A colour photosensor, for colorimetric RGB-like discrimination of different light wavelengths in different locations of the same device, having a MOSFET structure similar to that of the JFET sensor of claim **8**, but in which the 'top gate' metallic contact previously mentioned in claim **8** is replaced with a gate oxide and a corresponding top transparent metal gate unto which the necessary potential is applied so as to deplete completely the 'top gate' superficial channel region, and thus to perform the desired absorption within the said depleted region of a third wavelength range, i.e. the violet-blue (shortest wavelengths) end of visible spectrum, the resulting photogeneration of new free charge carriers leading to a variation in the potential of this MOS gate and therefore, in the current circulating throughout the channel between the 'source' and 'drain' terminals, respectively;

11. A colour photosensing detector with a structure made of multiple vertically stacked JFET devices combining bulk channels as well as a surface one and in which the 'top gate' region of a JFET would also include the channel and 'source' & 'drain' of the upper JFET, formed in a silicon substrate of a first conductivity type of low or moderate doping concentration, for spectrometric-like discrimination of multiple light wavelengths ranges in the same location, the detailed structure of the colour photosensor comprising:

a first doped region of a second conductivity type opposite the first conductivity type of the substrate, preferably formed by epitaxial growth unto the said substrate, the junction between this region and the substrate being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption of the red (longest wavelengths) end of visible spectrum within the said depleted region, and in which the bottom part of the junction realized in the substrate is identified as 'bottom gate';

a second doped region of the first conductivity type formed in the first doped region, the junction between them being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption of the yellow wavelength range of the visible light within the said depleted region, while at the same time between this second doped region and the said substrate a first channel is formed in the said first doped region, contacted at its ends by strongly doped regions of the same doping type as the first doped region which act as 'source' and 'drain', respectively, so that a current could flow between them and be modified by photoconductivity modulation arising from the absorption of the orange wavelength range of the visible light within the said first channel;

a third doped region of the second conductivity type formed in the second doped region, the junction between them being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption of the blue wavelength range of the visible light within the said depleted region, while between this third doped region and the said second doped region a second channel is formed in the said second doped region, contacted at its ends by strongly doped regions of the same doping type as the second doped region which act as 'source' and 'drain', respectively, so that a current could flow between them and be modified by photoconductivity modulation arising from the absorption of the green wavelength range of the visible light within the said second channel, and at the same time this third doped region also constitutes a third channel itself, being contacted at its ends by strongly doped regions of the same doping type as the third doped region which act as 'source' and 'drain', respectively, so that a current could flow between them and be modified by photoconductivity modulation arising from the absorption of the violet wavelength range of the visible light within the said third channel (which can also be identified for this device as the 'top gate' region);

a very deep and strongly doped diffused region of the same first conductivity type as the substrate, and of doping concentration much higher than that of the said substrate, necessary in order to contact the silicon substrate part of the 'bottom gate' of the multiple JFET structure from the front of the wafer;

an opaque region placed on top of the chip such that it allows the exposure to the incident light only of the photosensitive region of interest and the corresponding bulk regions underneath them, namely the central part of the 'top gate' and bulk channels, respectively;

the photocurrent sensors, or their equivalent electronic circuits, connected to each terminal in order to measure the photocurrents generated by the various wavelength ranges of the visible light in the said photodiodes, as well as the current values in and out of the said bulk and surface channels so as to detect the variation due to photoconductivity modulation, respectively.

12. A colour photosensing detector with a structure made of three vertically stacked JFET devices and in which the channels of the JFETs are separated from one another by strongly doped gate regions common to the adjacently neighbouring JFETs, formed in a silicon substrate of a first conductivity type of high or very high doping concentration, for spectrometric-like discrimination of multiple light wavelength ranges in the same location, the detailed structure of the colour photosensor comprising:

a first doped region of a second conductivity type opposite the first conductivity type of the susbtrate and of a very low doping concentration, formed by epitaxial growth unto the said substrate, the junction between this region and the substrate being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a first wavelength range of the visible light, i.e. light at the red (longest wavelengths) end of visible spectrum becomes absorbed in the photodiode thus formed, and in which the bottom part of the junction realized in the substrate is identified as 'bottom gate' (or 'gate 1');

a first buried layer of the first conductivity type and very strongly doped, locally diffused on an extended area on top of the said first doped region, to act as gate region ('gate 2') for both the bottom-most JFET structure realized in the first doped region and the one to be realized

in the region on top of it, so that the junction formed with the upper part of the first doped region is formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a third wavelength range of the visible light;

a second doped region, of the second conductivity type opposite the first conductivity type and of a moderate doping concentration, formed by epitaxial growth unto the said first doped region and the first buried layer diffused into it, the junction between this region and the said first buried layer being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a fourth wavelength range of the visible light, and in which the said first buried layer situated at its bottom ('gate 2') also acts as a gate for the JFET channel that would be realized within this second doped region;

a second buried layer of the first conductivity type and very strongly doped, locally diffused on an extended area on top of the said second doped region but of smaller length than the first one (although centered with respect to it), to act as gate region ('gate 3') for both the JFET structure realized in the second doped region and the one to be realized in the region on top of it, so that the junction formed with the upper part of this second doped region is formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a sixth wavelength range of the visible light;

a third doped region, of the second conductivity type opposite the first conductivity type and of a reasonably high doping concentration, formed by epitaxial growth unto the said second doped region and the second buried layer diffused into it, the junction between this region and the said second buried layer being formed at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a seventh wavelength range of the visible light, and in which the said second buried layer situated at its bottom ('gate 3') also acts as a gate for the JFET channel that would be realized within this third doped region;

a top-most fourth region layer of the first conductivity type and very strongly doped, diffused into the third doped region and which should be electrically connected to the second buried layer ('gate 3'), can be optionally included so as to form a junction with the upper part of the third doped region at such a depth, and reverse biased to generate a depletion region of such a width, so that these junction depth & depleted width values enable the absorption within the said depleted region of a ninth wavelength range of the visible light;

multiple 'source' and 'drain' regions, all of the same second conductivity type opposite the first conductivity type and strongly doped, diffused correspondingly at different (decreasing) depths in the first, second and third doped regions, respectively, in order to permit the flow of a drain-to-source current through the middle parts (nondepleted by top or bottom depleted regions generated by the buried layers) acting as channels of the JFETs realized in the said first, second and third doped regions, so that the drain-to-source currents flowing through them can be modified by photoconductivity modulation arising from the absorption of the second (shorter wavelengths than the first range), fifth and eighth wavelength ranges of the visible light within the said channels, respectively (in the case that the top-most fourth region is not included in the device structure, the absorption of the ninth wavelength range will also contribute to the photoconductivity modulation in the top-most channel within the third doped region);

multiple regions for gate contacts, all of the same first conductivity type and strongly doped of the buried regions , diffused correspondingly at different (decreasing) depths so as to contact the first buried layer, second buried layer and the substrate, respectively;

an opaque region placed such that its location and extension allows the exposure to the incident light of the photosensitive regions of interest and the corresponding bulk regions underneath them, namely the central part of the device centered in the middle of all the buried layers and the channels of all JFET transistors, respectively;

13. A deep trench structure for contacting any first region of a first conductivity type, situated at a certain depth from the surface and thus covered by a second region of a second conductivity type opposite to the first one, comprising:

a trench etched down to the depth necessary for the required purpose (e.g. the depth for contacting a certain region), that will etch and penetrate through the top second region;

a third region of the same first conductivity type and of high or very high doping concentration, diffused into the silicon after etching the trench at the required depth (e.g. diffused by a short thermal drive-in from a polysilicon layer deposited uniformly along the entire profile of the etched trench and *in-situ* doped with the suitable dopant so as to serve as doping source);

a thin oxide layer covering the walls of the said trench, grown thermally either before or after the deposition of the said polysilicon layer that serves as doping source, and which can be optionally included or not in the structure of the trench;

a thick polysilicon layer that completely fills in and then overgrows above the said etched trench, that is planarized using etch-back or CMP techniques before being patterned and contacted by metal.

14. A colour photosensing detector as in claim **11**, but with the following differences:

(i) the contact to the substrate and –if so desired– (only one of, or all) the contacts to each buried layer are realized not by diffused regions but using trench structures as in claim **12**, each of these trenches being etched to the corresponding necessary depth and using the appropriate dopant (of the first type, similar to that of the substrate);

(ii) the 'source' and 'drain' contacts for each JFET transistor within the structure, if so desired, can also be realized using trench structures as in claim **12**, etched to the corresponding necessary depth for each transistor and using the appropriate dopant (of the second type, similar to that of the first, second and third epitaxial regions, respectively).

15. A colour photosensing detector as in claim **11**, but with the following differences:

(i) the second (middle) and third (top-most) JFETs are now delineated by etching the corresponding epitaxial layer in which each of them is realized as well as those on top of it (if any);

(ii) the top-most fourth region layer, if desired to be included in the structure of the device, may be realized not by diffusion but by epitaxial growth, and can also be delineated into the desired shape at the desired location by etching it on top of the third epitaxial region;

(iii) the entire structure can be planarized using, e.g., thick oxide depositions followed by CMP and then sequential subsequent opening of the various diffusion and/or contact windows, although this planarization procedure may not always be necessary, its application necessity depending on both the exact thicknesses desired for each etched epi layer, and on the performance and features of the user's photolithographic process;

(iv) the drain and source contacts can now be all realized at the same time using strongly doped diffused regions of the same second doping type as that of the first, second and third epitaxial regions, respectively, so that all these 'drain' and 'source' contacting regions have the same final depth as realized after a processing consisting of photopatterning with a single mask defining the openings for all these regions, followed by implant and drive-in that result in a convenient depth of these contact regions;

(v) the contact regions for the buried layers ('gate 2' and 'gate 3' contacts) can now be all realized at the same time, using strongly doped diffused regions of the same first doping type as that of the substrate, all these 'gate' contacting regions have the same final depth as realized after a processing consisting of photopatterning with a single mask defining the openings for all these regions, followed by implant and drive-in that result in a convenient depth of these contact regions;

(vi) the contact region for the substrate ('gate 1' contact) is realized not by using a deep diffused region but using a trench structure as in claim **12**.

16. A colour photosensing detector as in claim **13**, with the difference that all the 'source' contact regions/trenches are now confounded in a single common 'source' contact region/trench, of the same depth as the contacting region for the 'drain' contact region/trench of the bottom-most JFET transistor (which has its channel in the first epi region of the second doping type and very low doping concentration), which automatically implies that the pattern of the buried regions must be situated at a certain safety margin distance from the estimated final edge of this common 'source' contact region/trench.

17. A colour photosensing detector as in claim **15**, with the difference that only one common 'gate' region is now implemented by extending the buried layers along one axis to the same width so that they touch and are confounded with the deep region/trench contacting the substrate, thus ensuring a single 'gate' contact for all the JFET transistors in the triple vertically stacked structure of the photosensor, and therefore resulting in a small element highly suitable for usage as elementary pixel in imaging arrays (together with the correspondingly necessary row & column addressing circuits as well as other signal processing circuitry that can be placed either in a non-illuminated part of the same pixel, or in a different location of the same chip).

18. Colour photosensing detectors as in claims **15** and **16**, but with the difference that etching-based delineation of each JFET transistor in the structure can also be additionally included in the processing required to realize their respective structures.

19. A colour photosensing detector with a FCT-like structure, formed in a silicon substrate of a first conductivity type of high or very high doping concentration, for colorimetric discrimination of multiple light wavelength ranges in the same location with electrical tunability of the spectral characteristic, the detailed structure of the colour photosensor comprising:

a first doped region of the first conductivity type and of very low or low doping concentration, preferably formed by epitaxial growth unto the said substrate (which can be identified as the 'cathode'),

a second doped region of a second conductivity type opposite the first conductivity type and of very high doping concentration, which can be identified as the 'gate', formed in the first doped region by using either deep diffusion or trench structures as in claim **12** and of the corresponding correct doping, and placed in either two lateral locations or in an annular/polygonal shape that surrounds the central part of the device, with a large depth of penetration that extends a considerable way throughout most of the first epi region and is also much larger than its width, connected via a first bias resistor of very high value to a first external bias supply which reverse biases the junction formed between this second region and the said first epitaxial region, therefore leading to the development of depleted regions that extend laterally within the central part in the first epi region and along the vertical walls of this/these second region(s);

a third doped region of a second conductivity type opposite the first conductivity type and of high or very high doping concentration, which can be identified as the 'anode', formed in the first doped epi region in a central location symmetrically located inside the area delimitated by the second region, with a relatively shallow junction, connected via a second bias resistor of relatively high value to a second external bias supply which reverse biases the junction formed between this third region and the said first epitaxial region, therefore leading to the development of a depleted region that would by default extend downwards within the central part in the first epi region, but which, due to the existence at the same time of the depleted region(s) developed laterally along the vertical walls of the second region(s) in a part of the same central location, will not be able to extend freely at the desired depleted width and therefore is compelled to compensate for the areas that were already occupied/depleted by the depleted region(s) of the second region(s) by extending downwards to a much larger extent than it would do normally only under the influence of the voltage of the reverse bias, thus resulting in different dependencies of the extensions of this depleted region width as a function of the extensions of the lateral depleted regions' width when the second bias supply

value is varied, i.e. resulting in different spectral characteristics when either the second bias supply value is held fixed and the first bias supply value is varied as a control parameter (preferred configuration) to adjust the spectral characteristic of the signal output collected from the third doped region, or viceversa;

a metallic contact at the bottom of the wafer to contact the 'cathode', or –if so preferred– contacting the bottom part of the silicon substrate from the front of the wafer using either a deep and strongly doped diffusion of the same first conductivity type as the substrate, or a trench structure as in claim **11** and of the corresponding correct doping;

an opaque region placed on top of the chip such that it allows the exposure to the incident light only of the photosensitive region of interest, namely the central part (the 'anode') of the device and the corresponding bulk region underneath it, respectively;

the photocurrent sensors, or their equivalent electronic circuits, connected to the terminals of interest in order to measure the photocurrents generated by visible light incident upon the device, e.g. one which measures the photocurrents generated in the lateral depleted regions developed by the deep vertical 'gate' and one which detects the photogenerated signal by picking up the voltage drop appearing across the second bias resistor under illumination and then subtracting from it the value corresponding to the non-illuminated case (by employing either a digital or analog memory, or a subtraction circuit which is also fed with a similar signal from a reference device identical with the used photosensors but unexposed to light), respectively.

20. A colour photosensing detector as in claim **18**, with the difference that the 'anode' region is patterned in such a way that merges with the deep lateral 'gate' regions, effectively resulting in a unique electrode (which can be identified in this case as 'anode-gate') that is connected via a single biasing resistor to an external bias supply that reverse biases the junction formed with the first epi region, so that the depleted region developed in the central region will still extend downwards more than it is theoretically supposed to because there still exist lateral extensions of the depleted region along the vertical walls that impede its free expansion, therefore resulting in a quick and easy variation of the spectral characteristic for the absorption in the central part of the device as a function of the applied bias value, variation that is consequently much faster and accentuated than in the case of a simple diode with the same parameters like the 'anode' shallow region but without the lateral deep 'gate' regions.

21. An active pixel imaging array, comprising:

(a) a matrix of rows and columns of colour photosensing detectors with a FCT-like structure, formed in a silicon substrate of a first conductivity type, for colorimetric discrimination of multiple light wavelength ranges in the same location with electrical tunability of the spectral characteristic, with each colour sensing pixel being a photodetector as in claim **19** but arranged such that the array structure is as follows:

(j) The 'gate' regions, realized as second doped regions of the second conductivity type formed in the epitaxially grown first doped region, are merged together in a rectangular (or other convenient polygonal) pattern and contacted with a single common electrode that is connected via a first bias resistor of very high value to a first external bias supply which reverse biases the junction formed between this third region and the said first epitaxial region, therefore leading to the development of depleted regions that extend laterally within the central part in the first epi region and along the vertical walls of this second region;

(ii) The 'anode' regions, realized as third doped regions of the second conductivity type formed in the epitaxially grown first doped region, are are separately and individually addressable for each pixel;

(iii) A 'cathode' region unique for the entire array, that contacts the bottom part of the silicon substrate from the front of the wafer using either a deep and strongly doped diffusion of the same first conductivity type as the substrate, or a trench structure as in claim **12** and of the corresponding correct doping;

(b) for each pixel in the said matrix, row and column select circuitry for selectively and subsequently switching each pixel 'anode' to a single common electrode that is connected via a second bias resistor of relatively high value to a second external bias

supply which reverse biases the junction formed between this third region and the said first epitaxial region, therefore leading to the development of depleted regions that extend downwards, within the central part in the first epi region and to a depth as compelled by the lateral extension of the depleted region width along the vertical walls of the second 'gate' region(s), as well as circuitry for reading or collecting the output signals representative of the colour information collected across/through the first and the second bias resistors, respectively, all this circuitry being placed either totally or partially in the pixel itself (next to the sensor but not exposed to incident light) and/or with the rest (or the whole) of the signal processing circuitry placed on the same chip but in another area of the device next to the array;

(c) multiple opaque regions placed such that their location and extension allows the exposure to the incident light only for the photosensitive regions of interest and the corresponding bulk regions underneath them, namely the central parts of the 'anode' regions of each pixel, respectively.

Fig. 3

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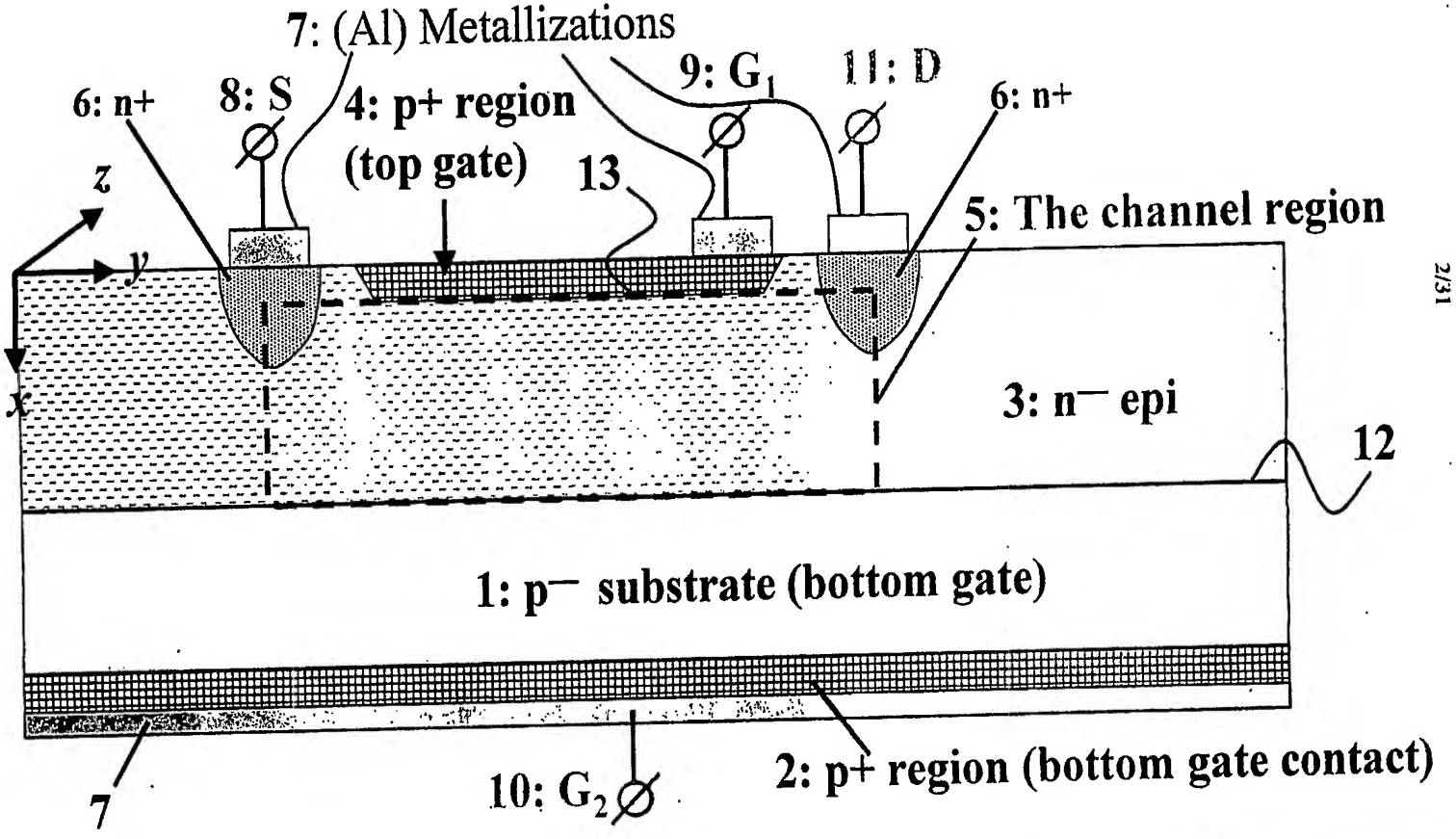
Fig.31:

Our Proposed ... RS

A) JFET-based (horizontal channel):

A.1) BULK channel

A.1.1) Single Device: Simplified schematic structure



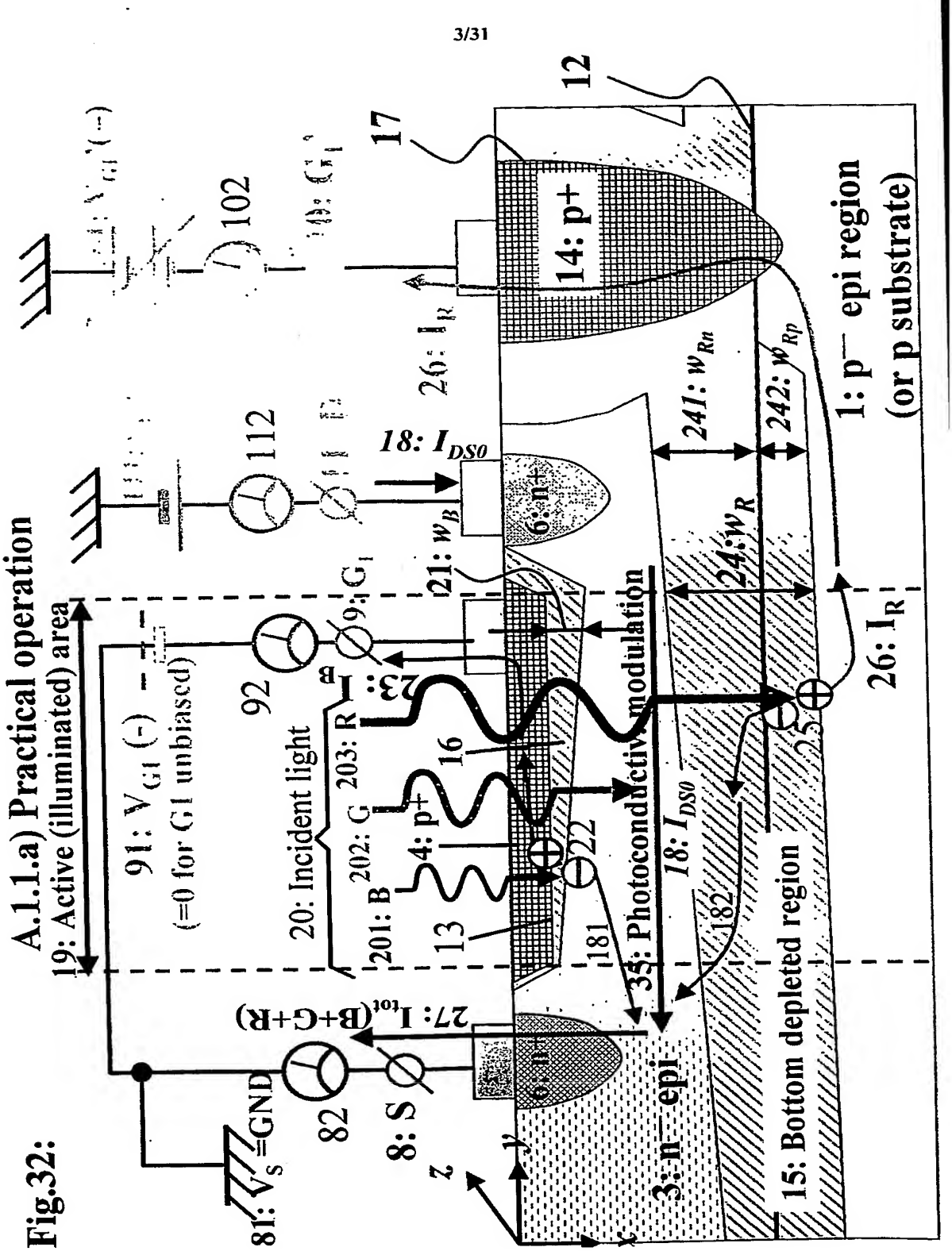


Fig.32:

Fig.33: **A.1.1.b) Practical operation: Buried layer version**

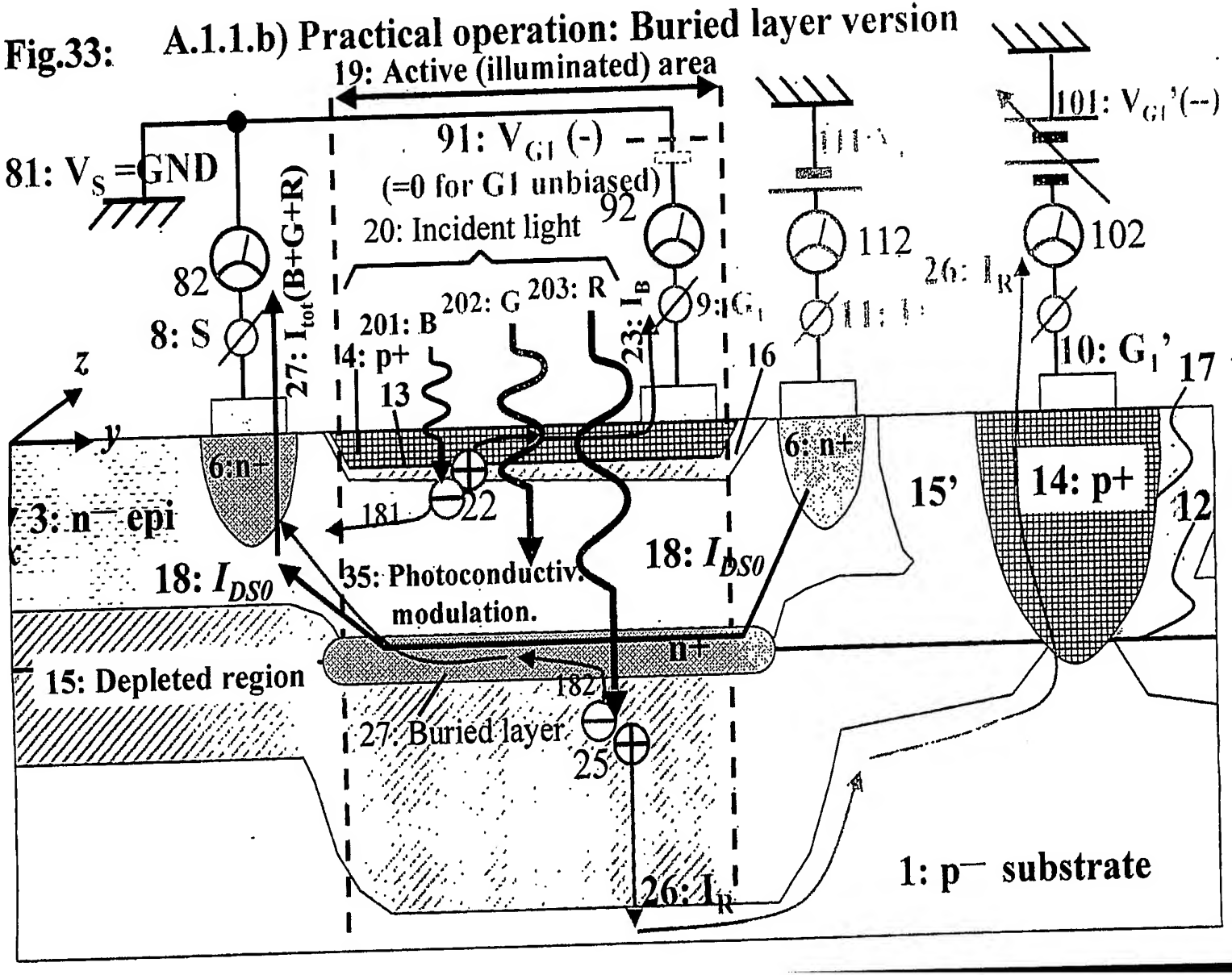


Fig.34-a: **A.1.2. Imaging *array* based on JFET photosensors:**
a) Structure of the 'compact' type of array;

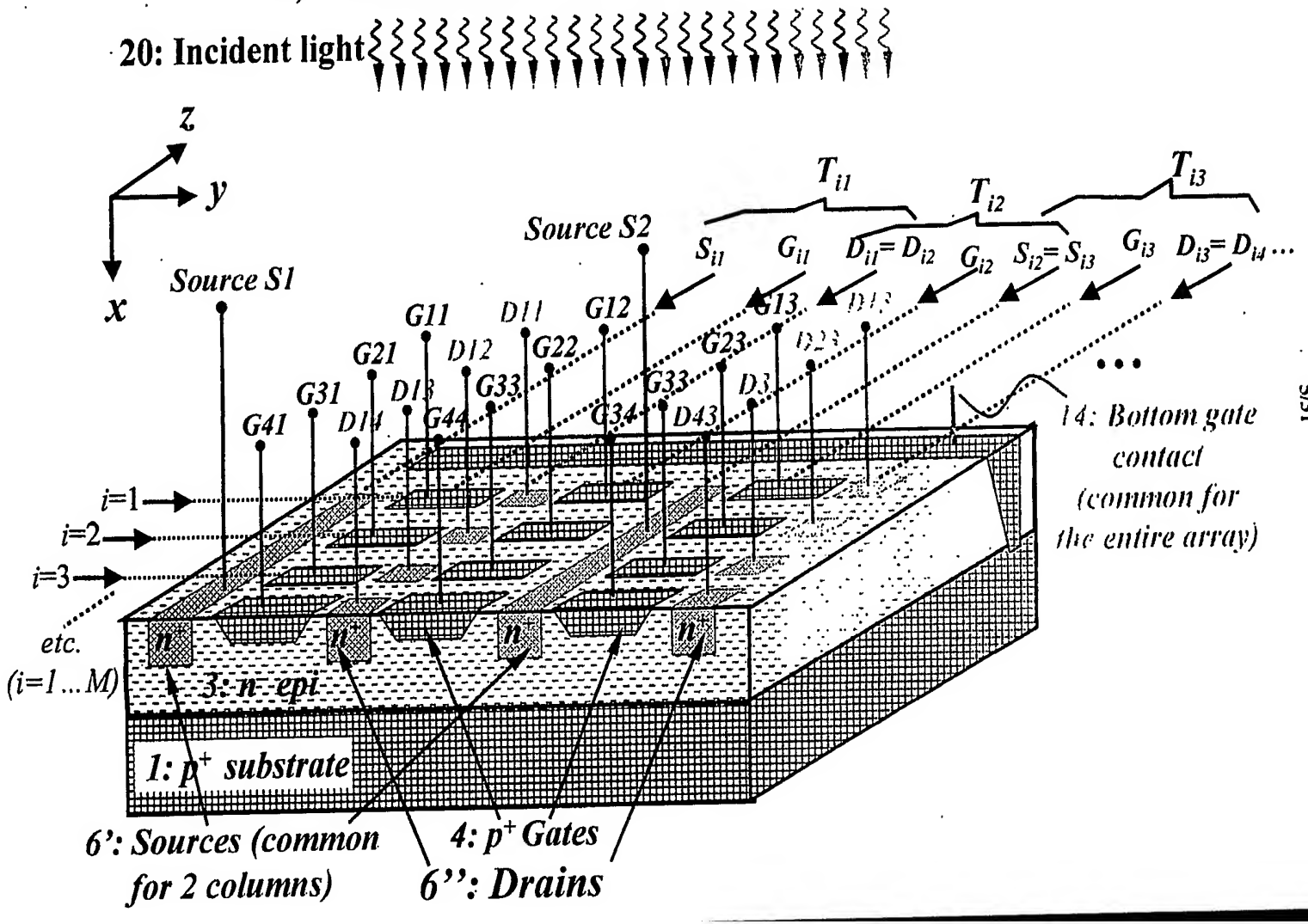


Fig.34-c: **A.1.2. Imaging *array* based on JFET photosensors:**
b) With separate bottom gate electrodes

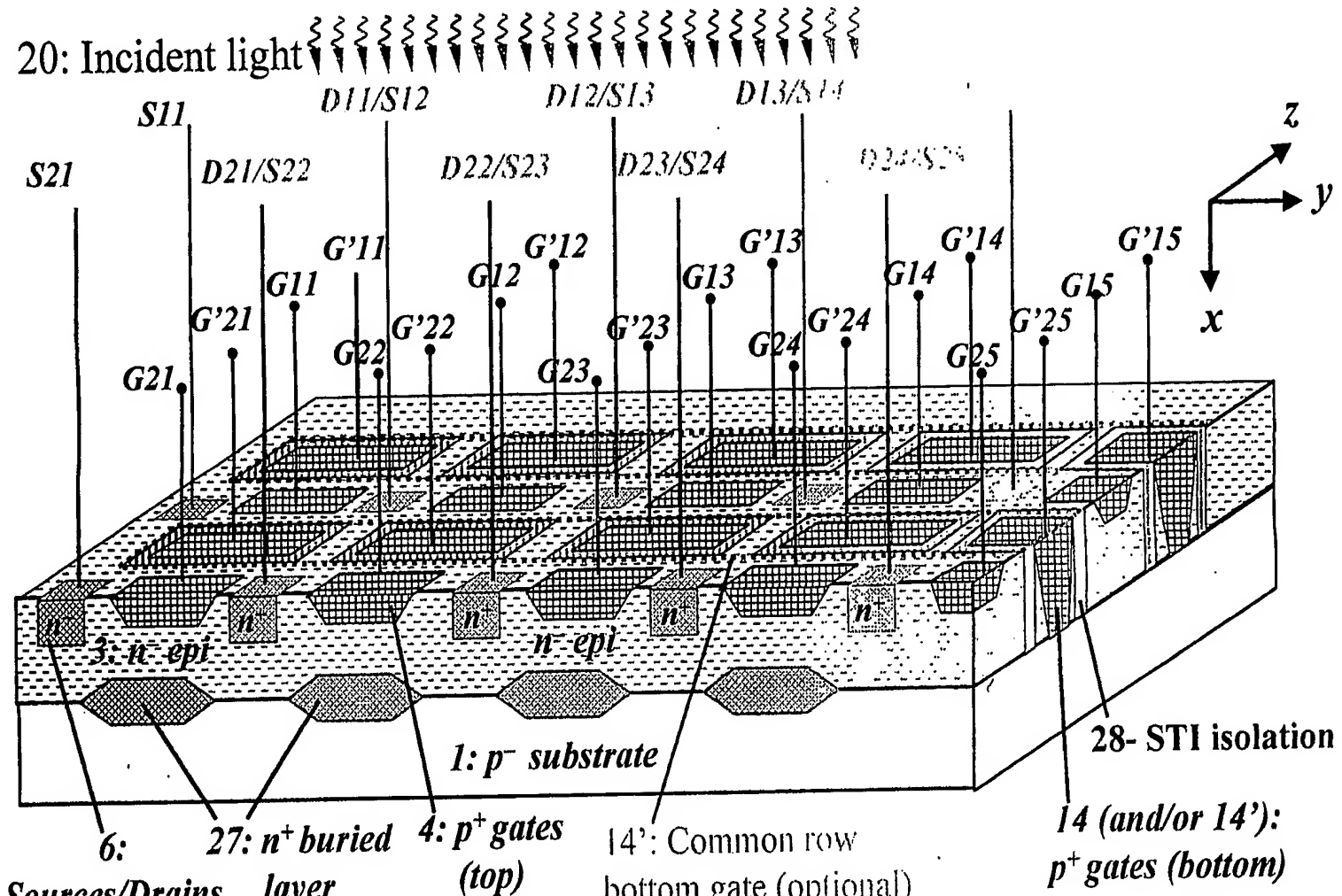
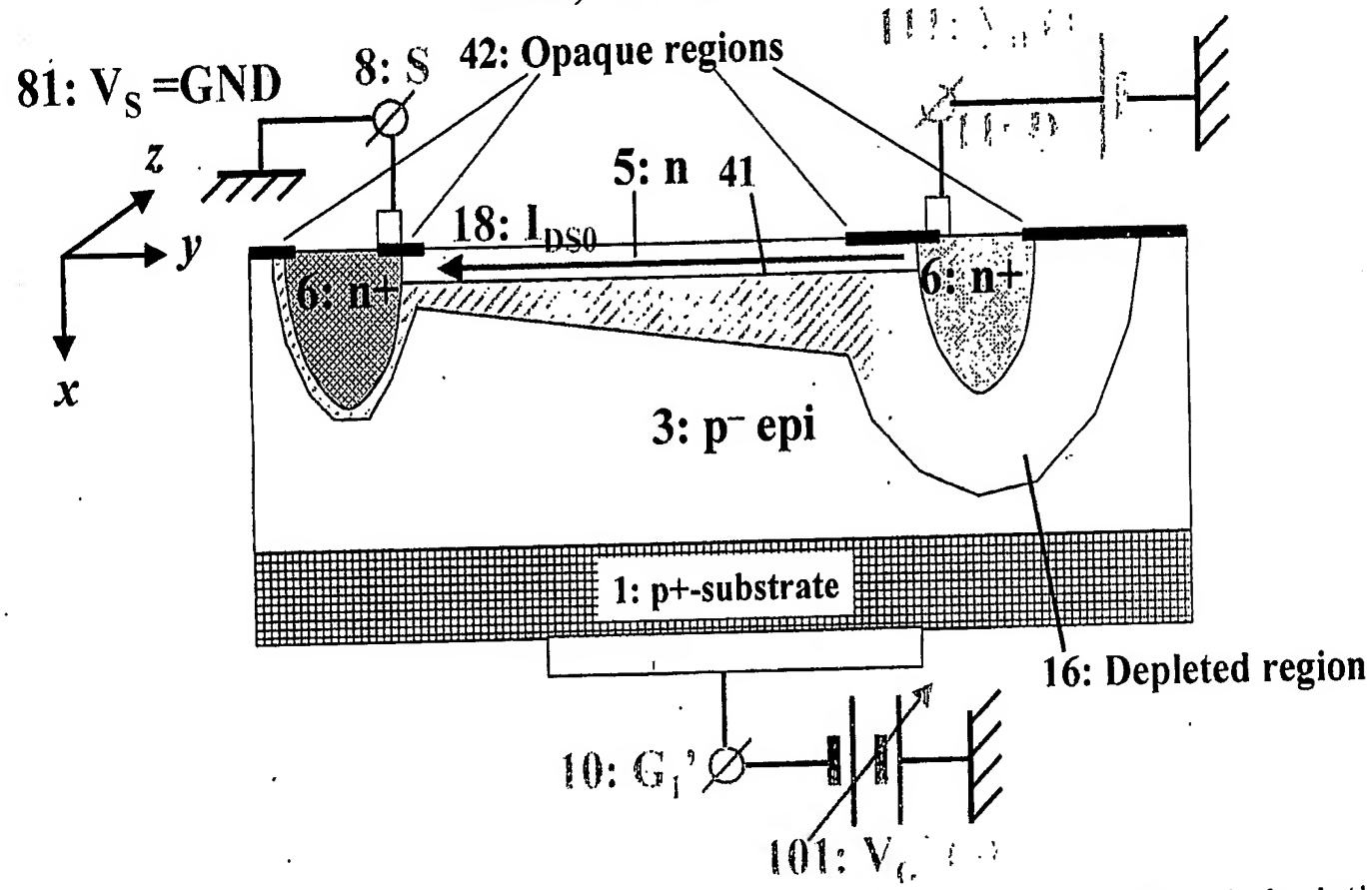


Fig.35: A) JFET-based

A.2) SURFACE channel

A.2.1) Basic structure (stand-alone device)



Drawbacks: lateral extension of depleted region; nonuniform width of depletion layer along the *n* channel; difficulty in collecting the photocurrent along the *n* channel

A.2.2) SURFACE channel imaging device providing simultaneous multiple outputs at collection (current measurement) electrodes

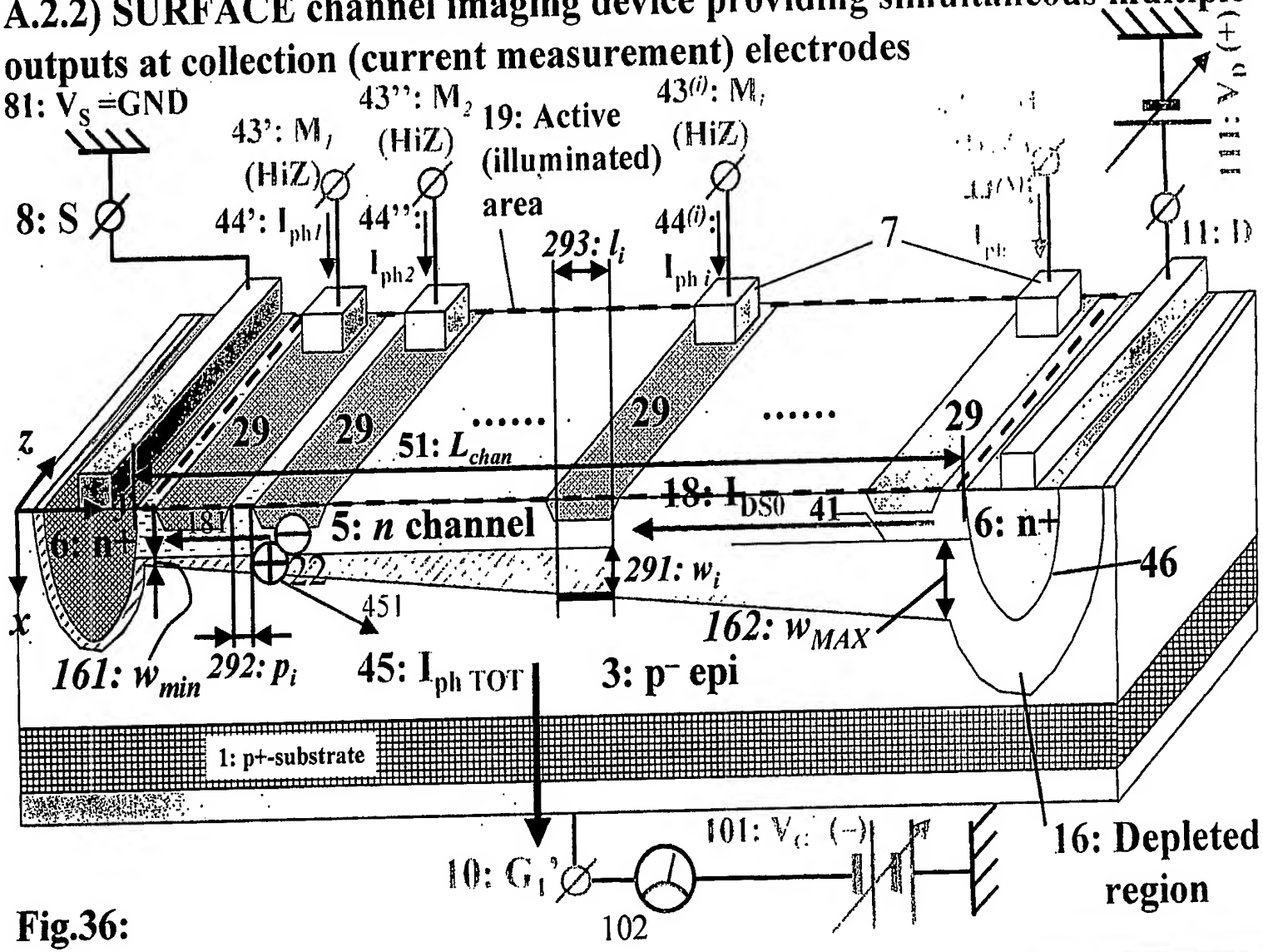
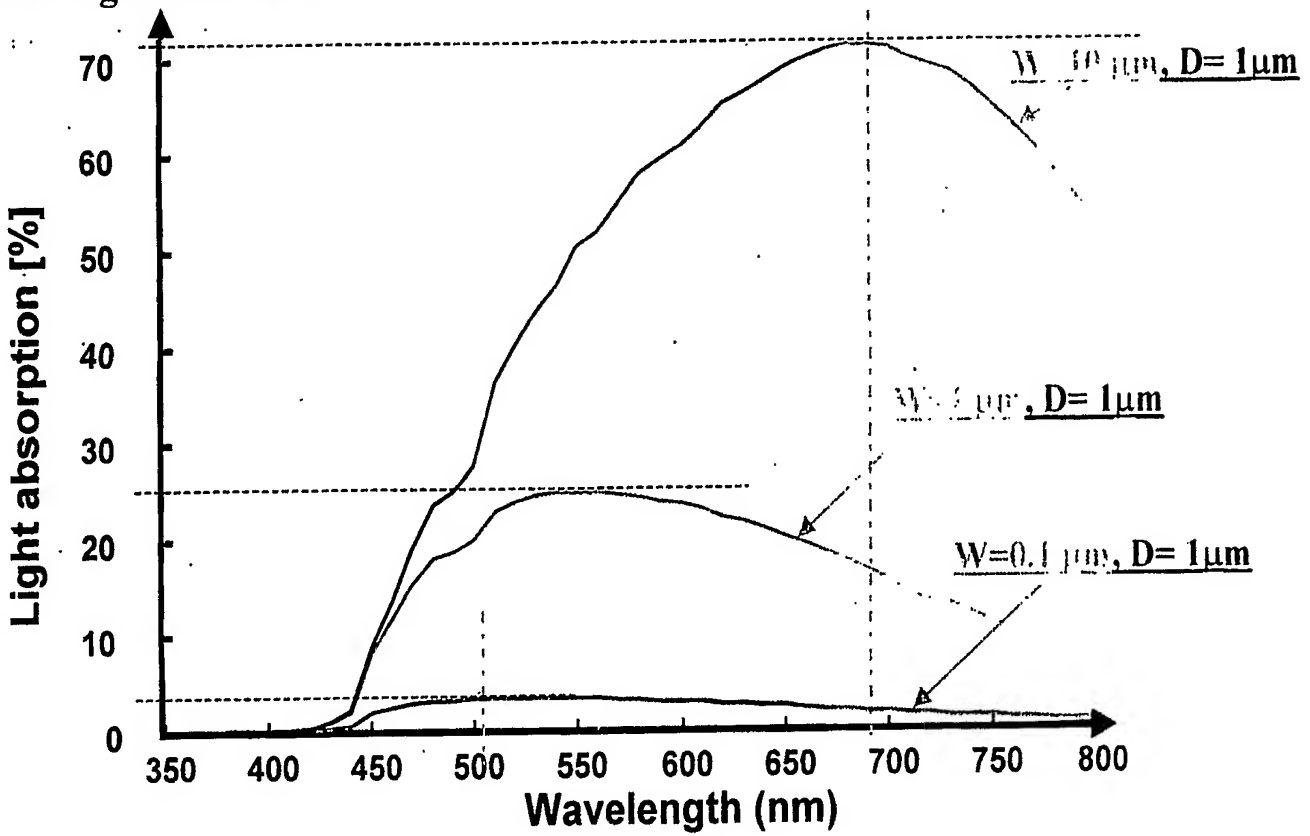


Fig.36:

Fig.37-a: Absorption of light in junctions of constant depth (D= 1μm) but with different depleted region widths *w*



Spectral response effects manifested due to an increasingly wider depletion region:

1. Variation of intensity of light absorption
2. Shifting of peak values
3. Bandwidth change

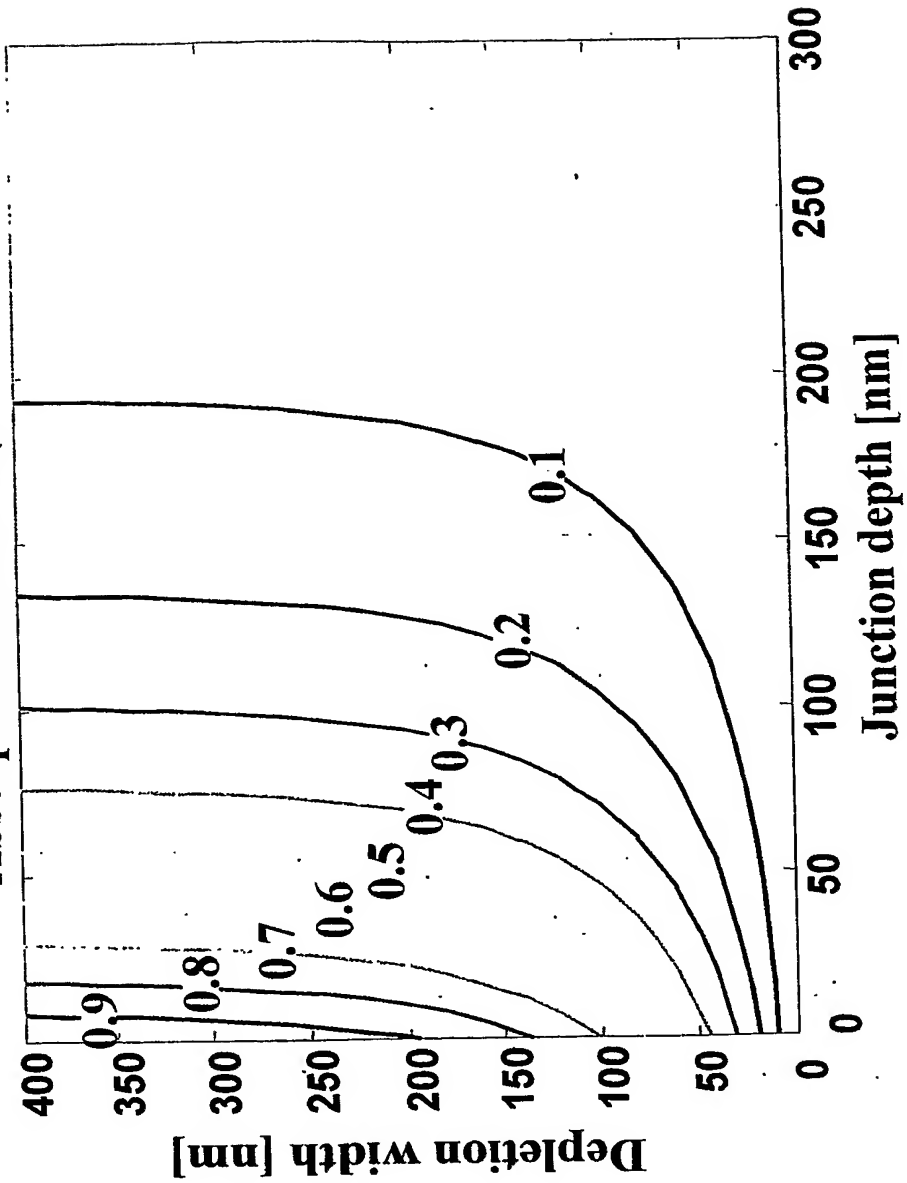


Fig.37-b: Light absorption in shallow junctions of different depth and with different depleted region widths w, for light with wavelength λ=400 nm

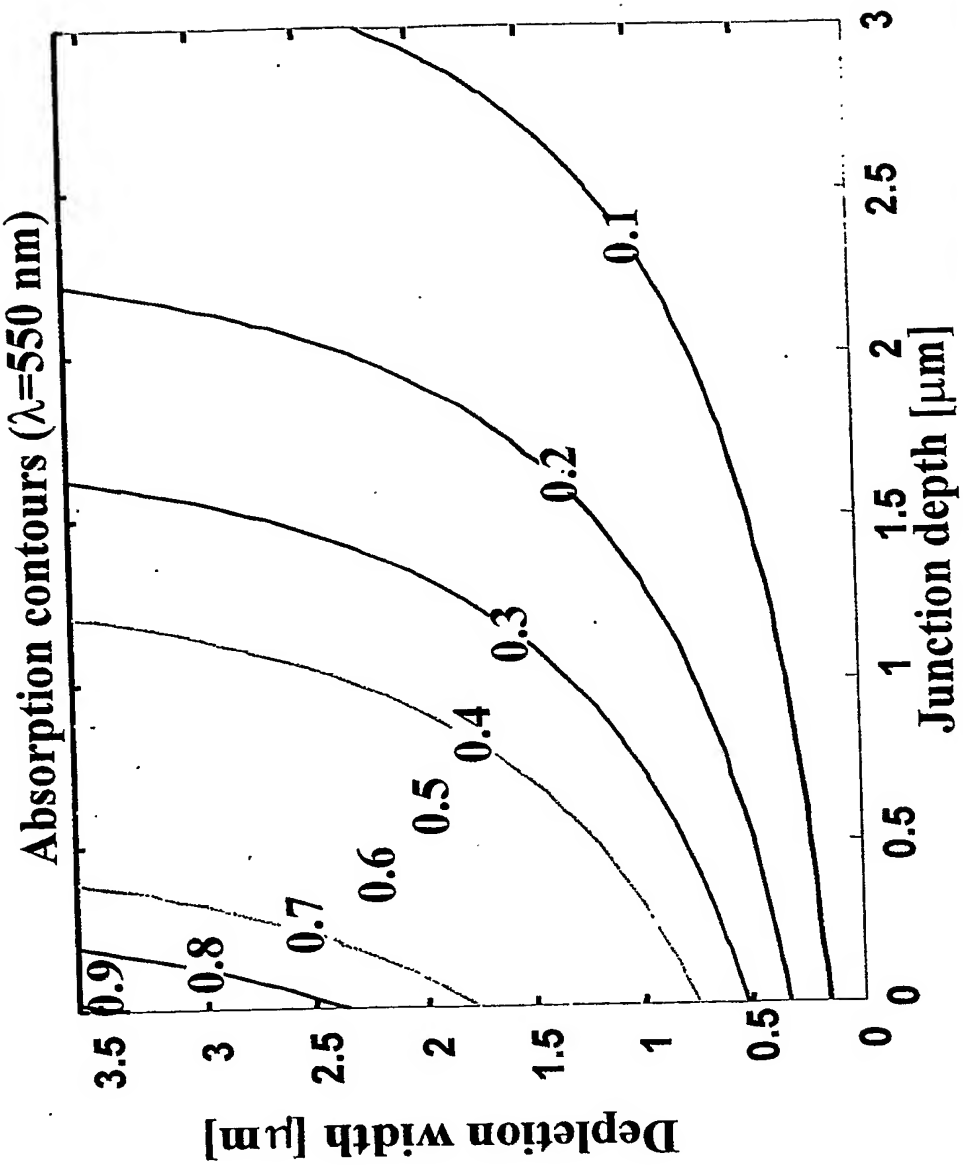
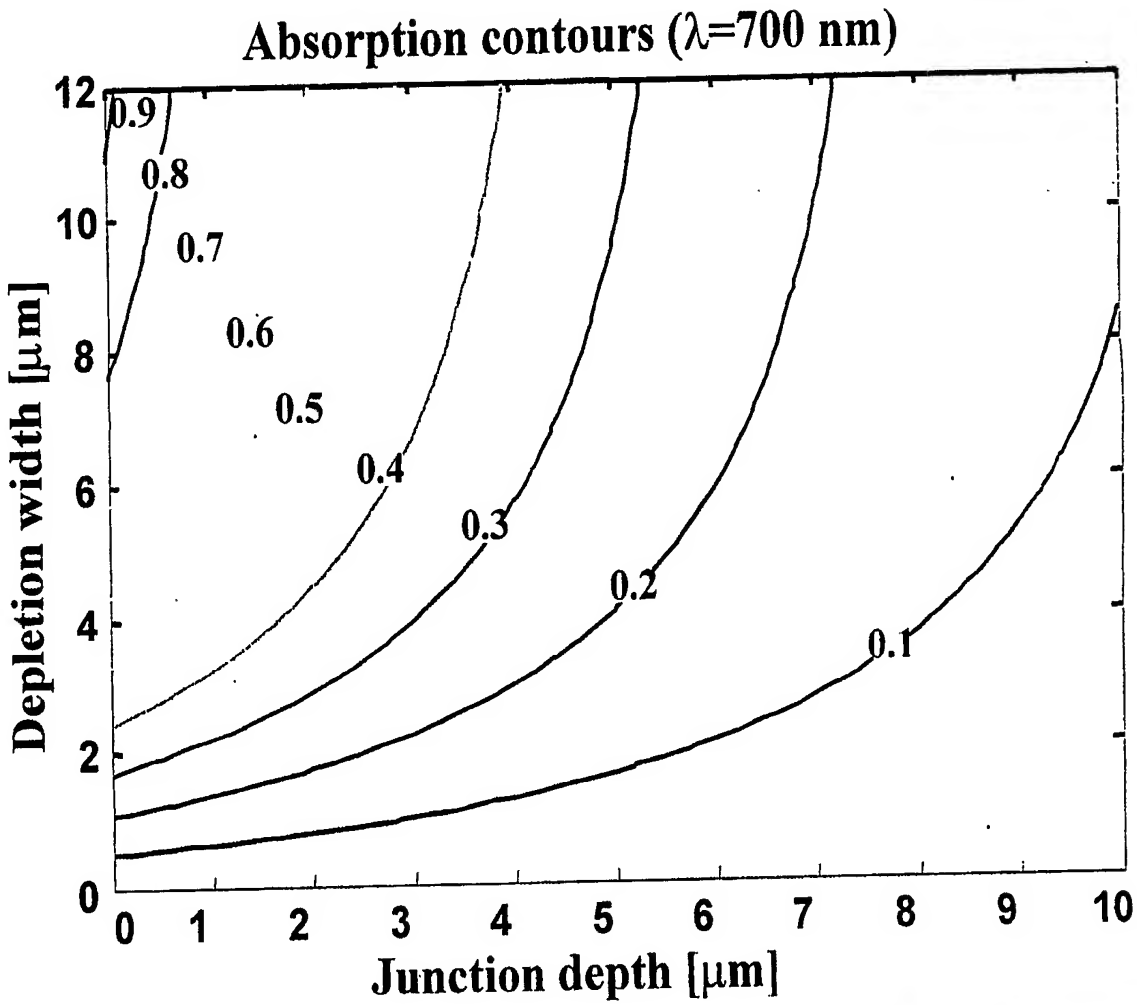


Fig.37-c: Light absorption in medium-depth junctions with different depleted region widths ν, for light with wavelength λ=550 nm

Fig.37-d: Light absorption in deep junctions with different depleted region widths *w*, for light with wavelength λ=700 nm



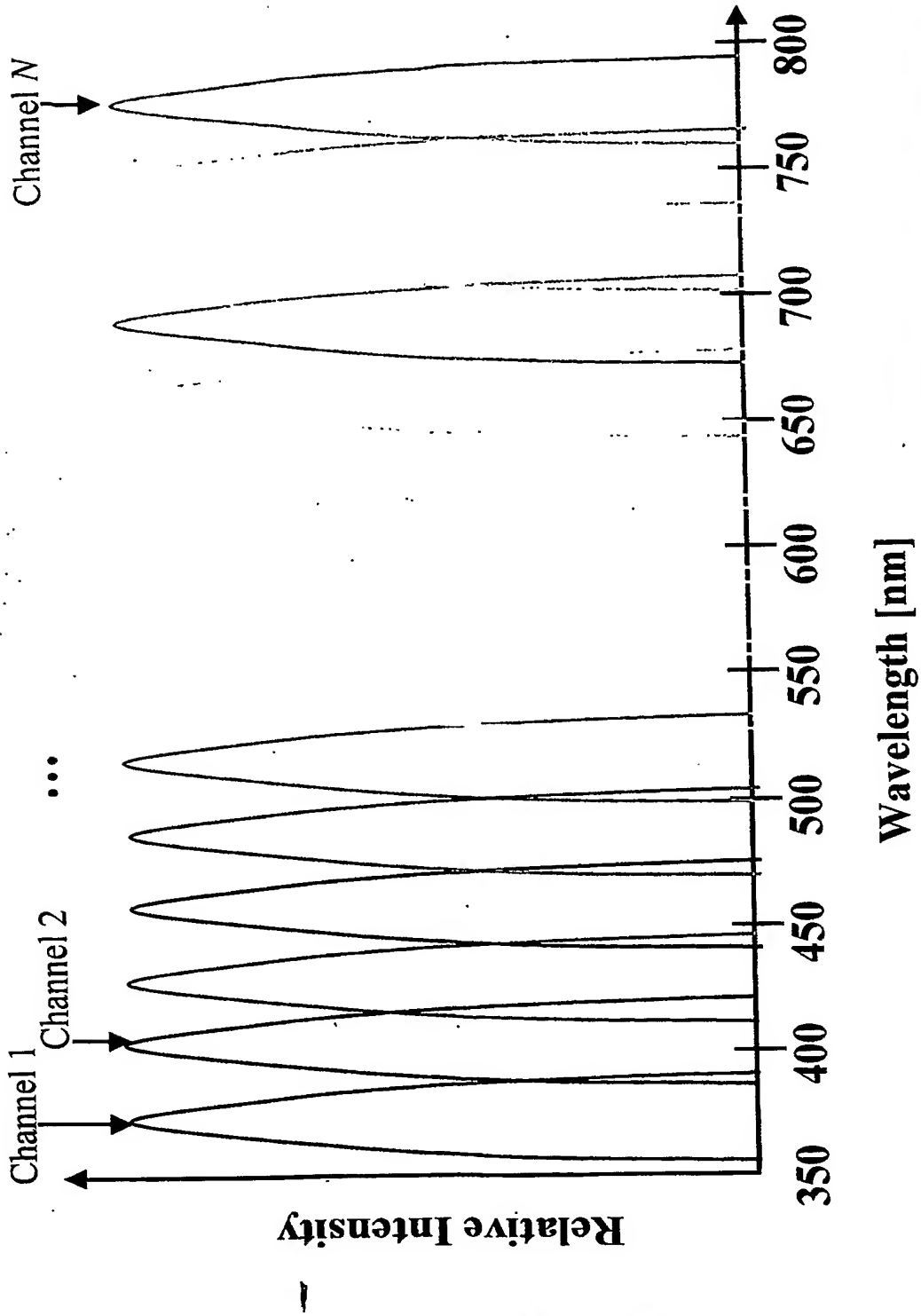


Fig.38: Example of spectrometric separation of light into multiple narrow-passbands.

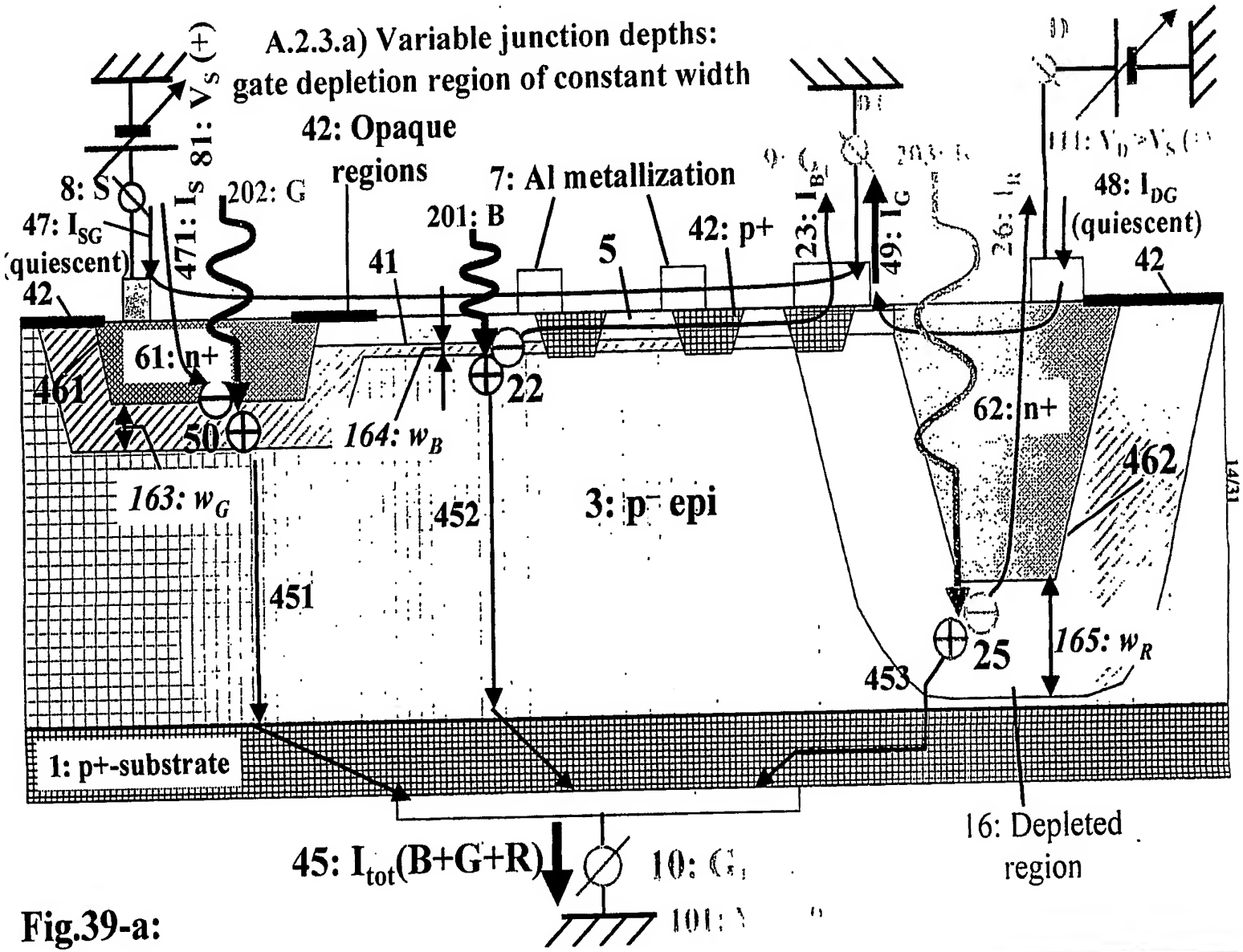


Fig.39-a:

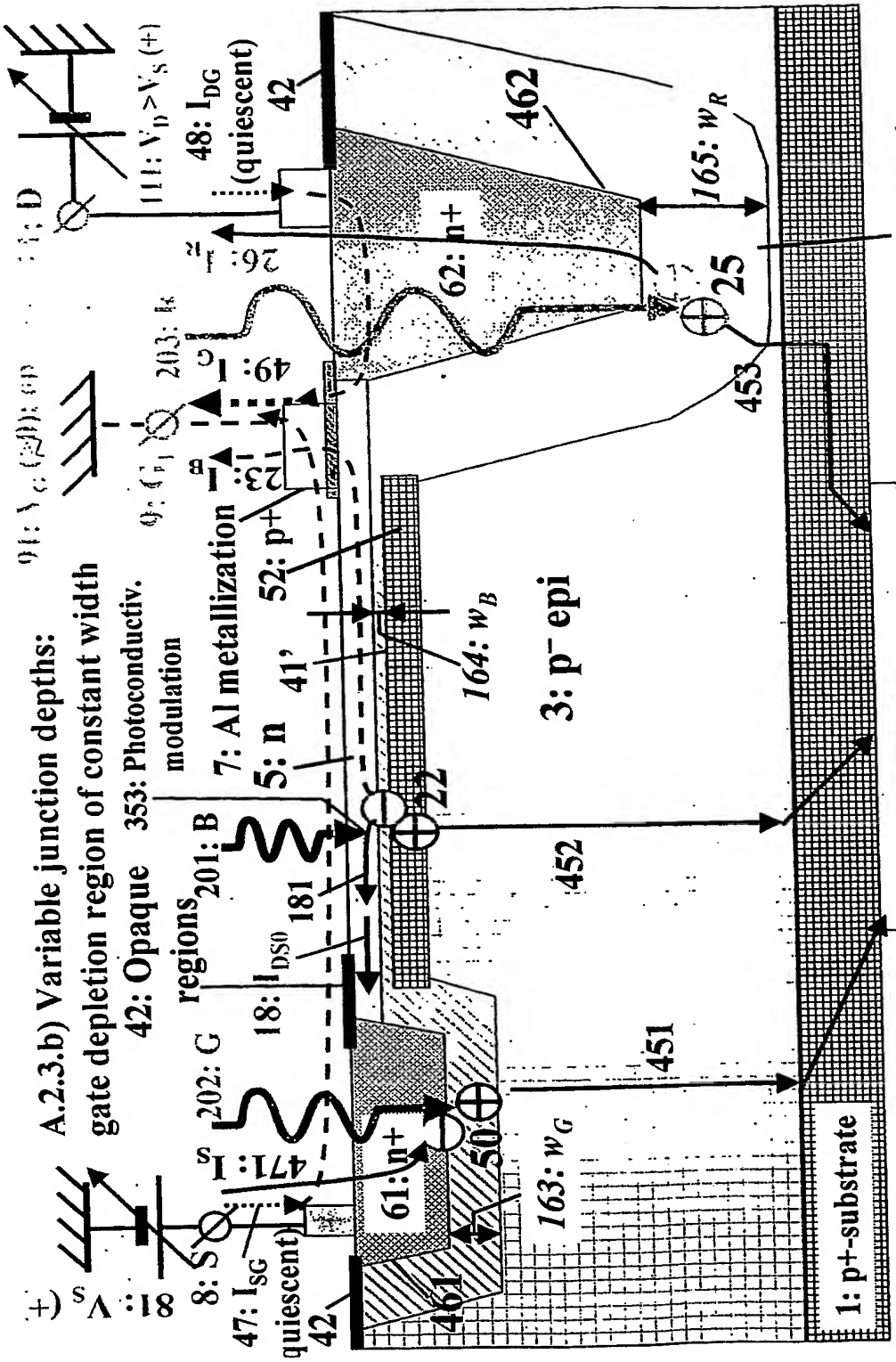


Fig.39-b:

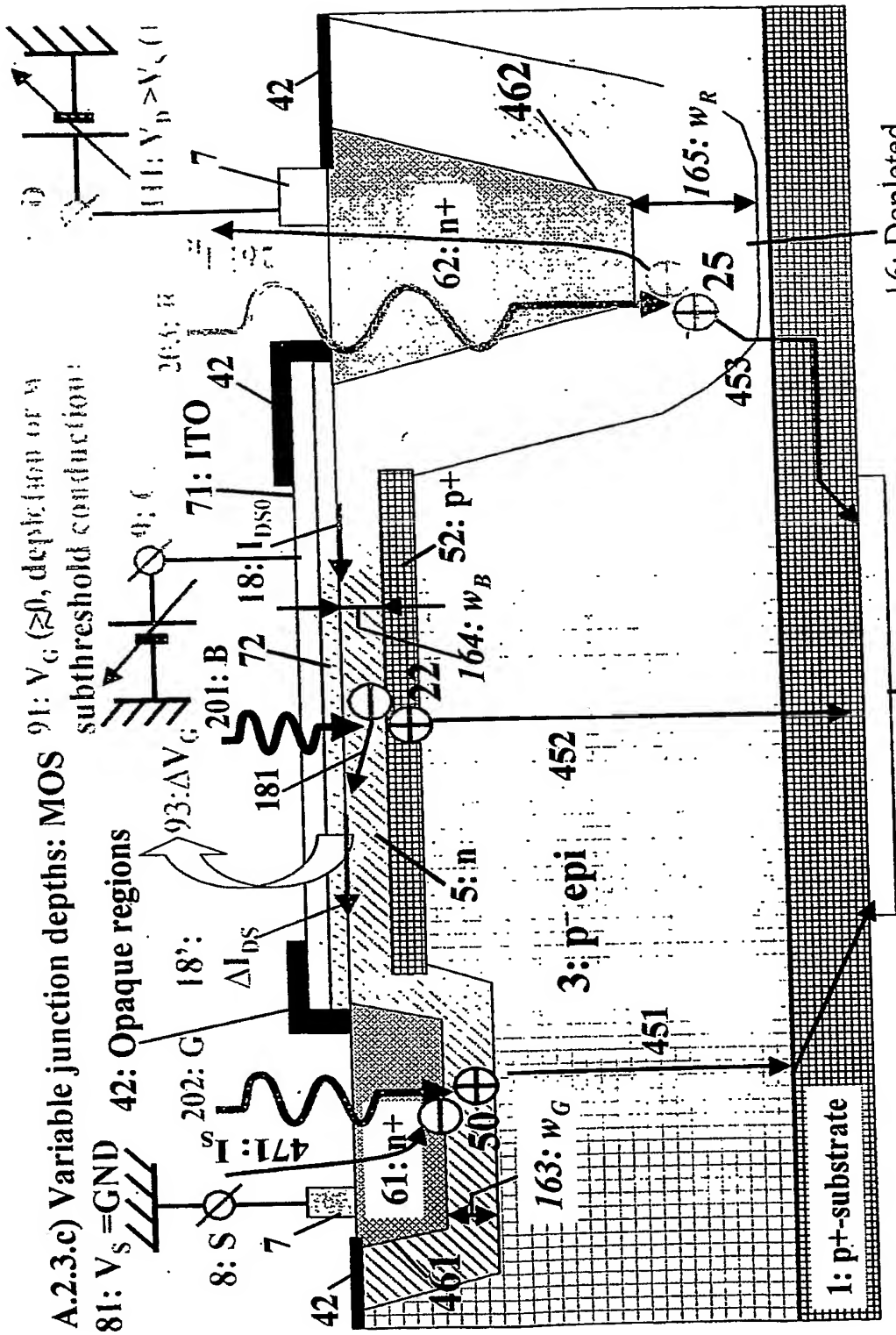


Fig.39-c:

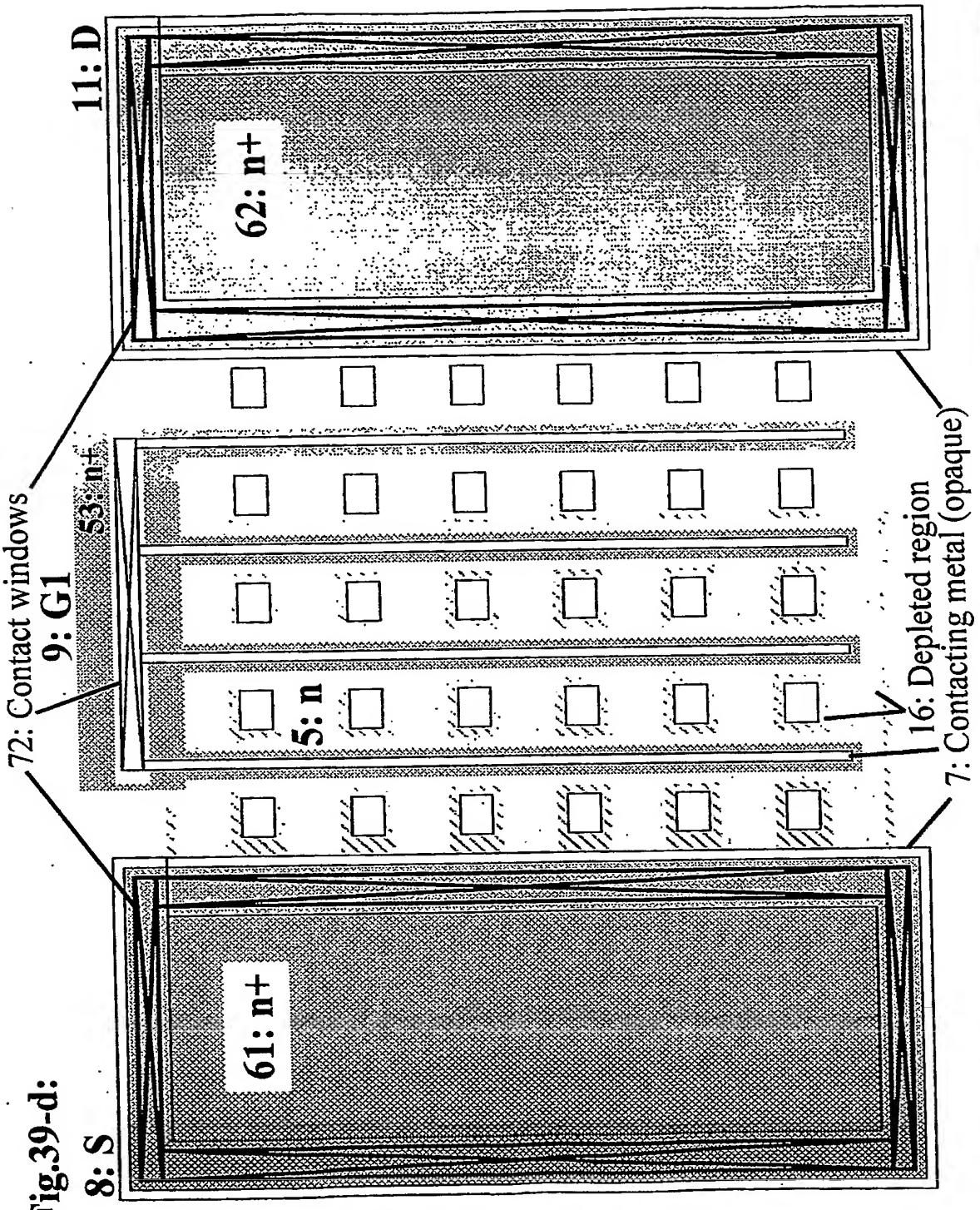


Fig.39-d:

Fig.40: A.3) Triple JFET (bulk AND surface channels) imaging device: a) Compact (G_i=D_{i+1})

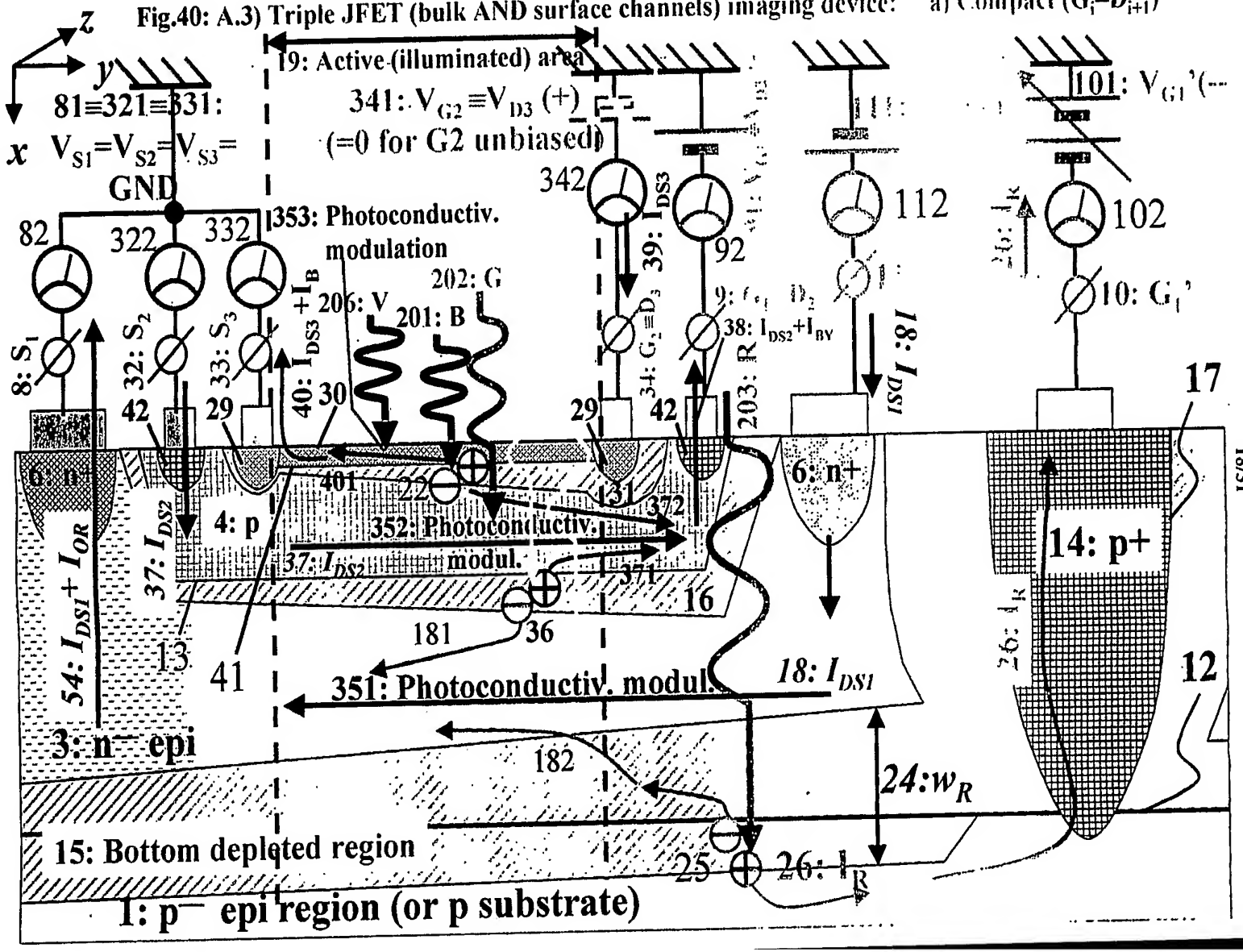
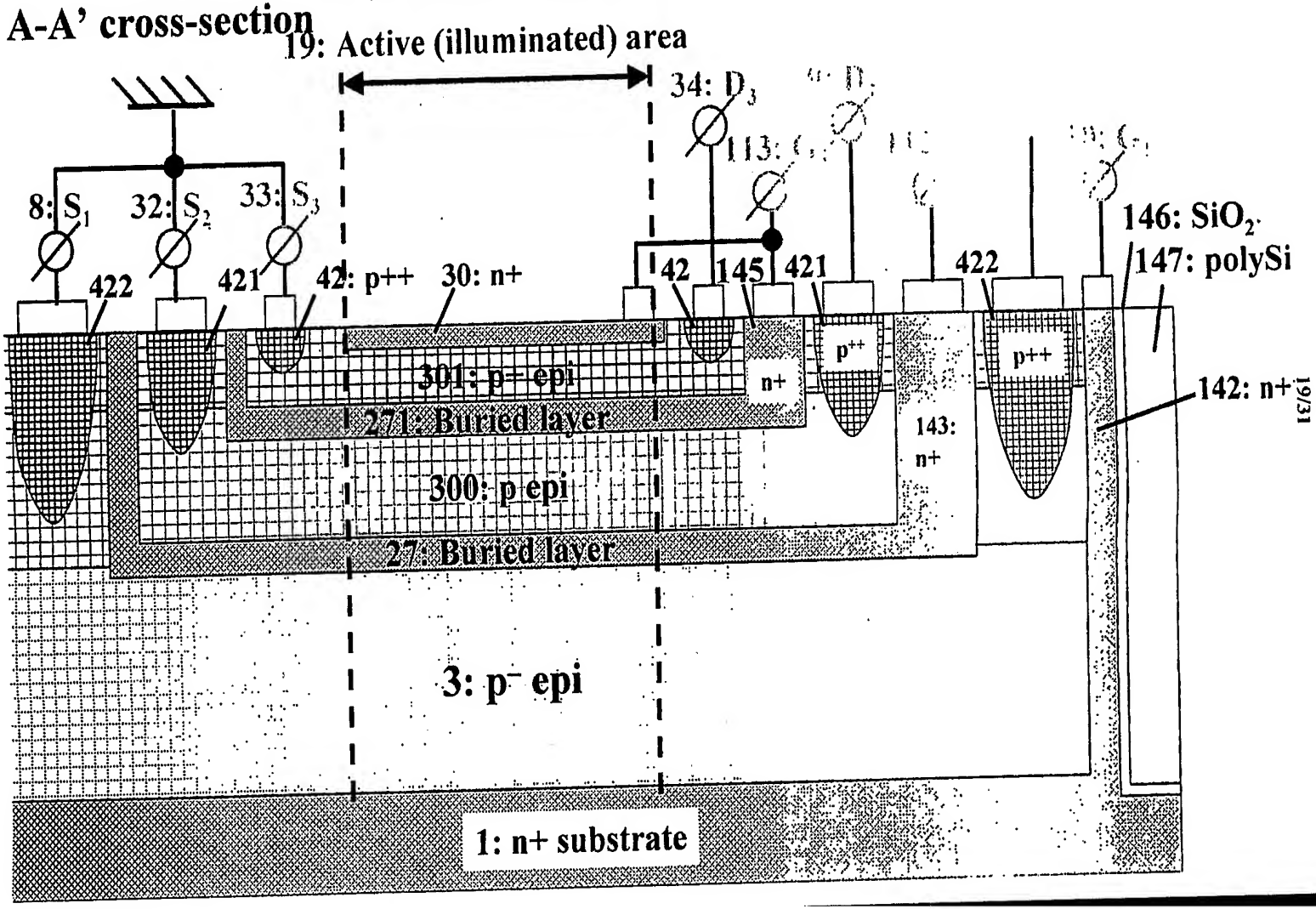


Fig.41-a: A.3) Triple JFET (bulk AND surface channels) imaging device
b.1) Separate channels and independent terminals



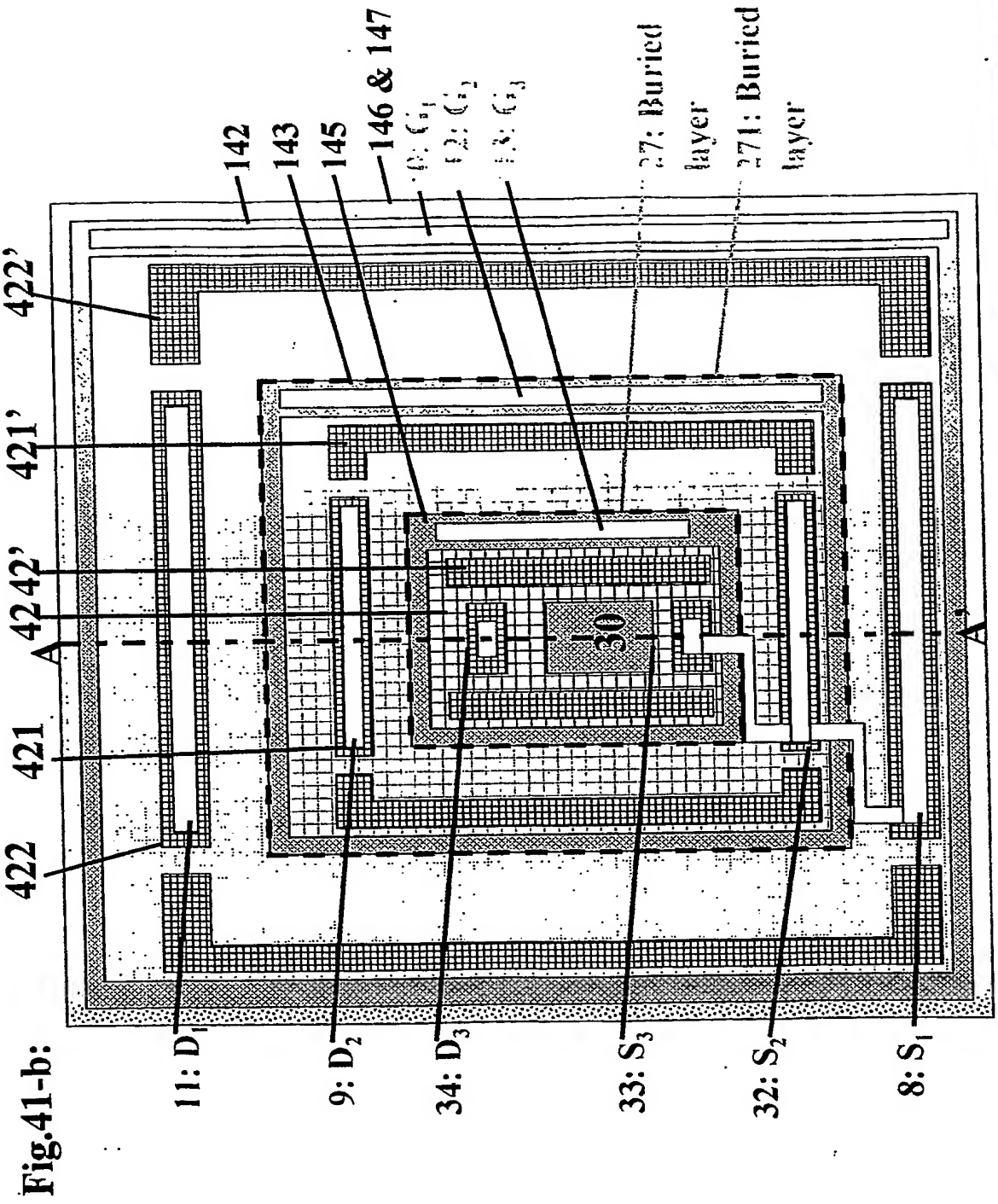


Fig.41-b:

Fig.42-a: A.3) Triple JFET (bulk AND surface channels) imaging device
b.2) Separate channels and independent terminals - etched delineation

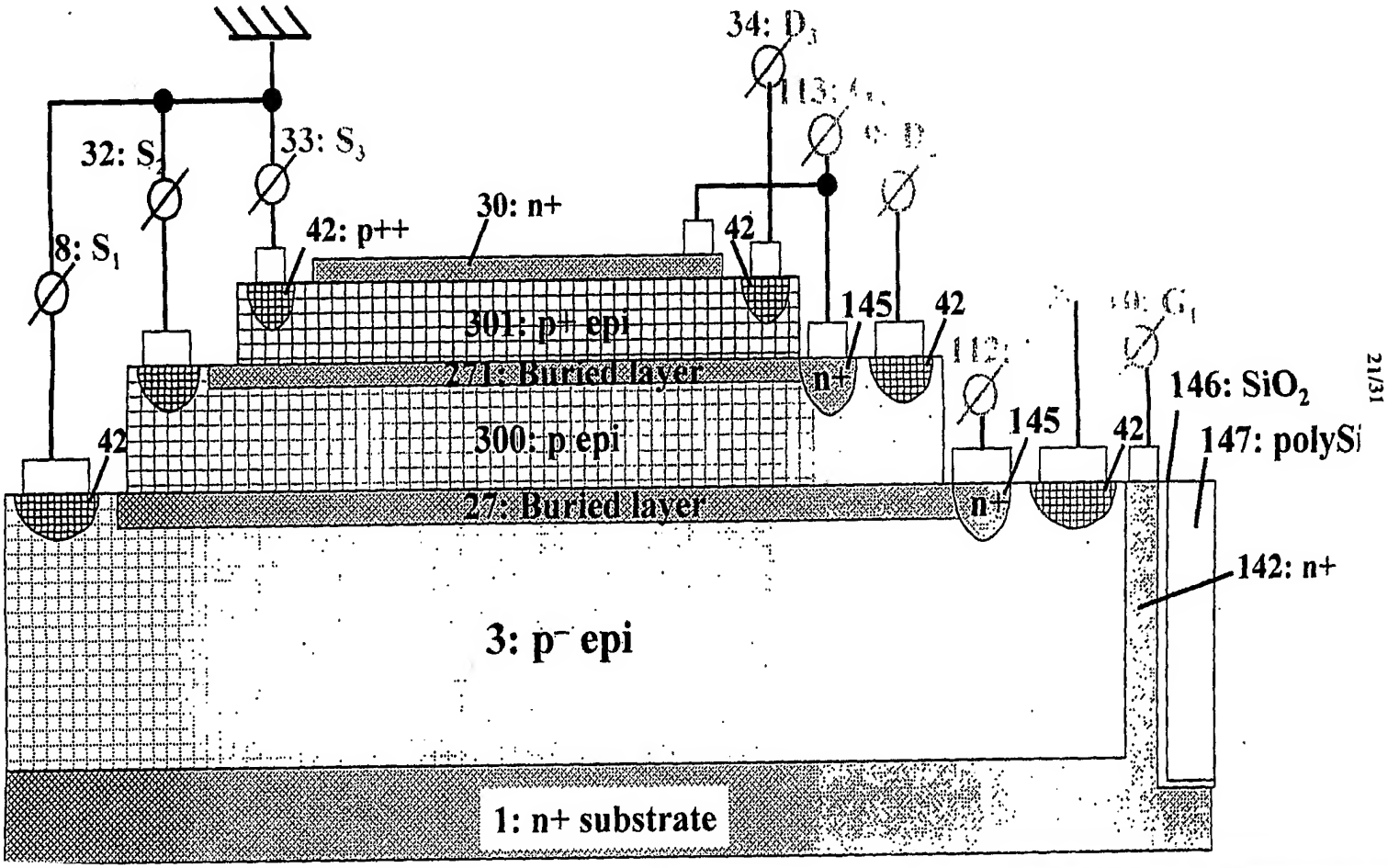
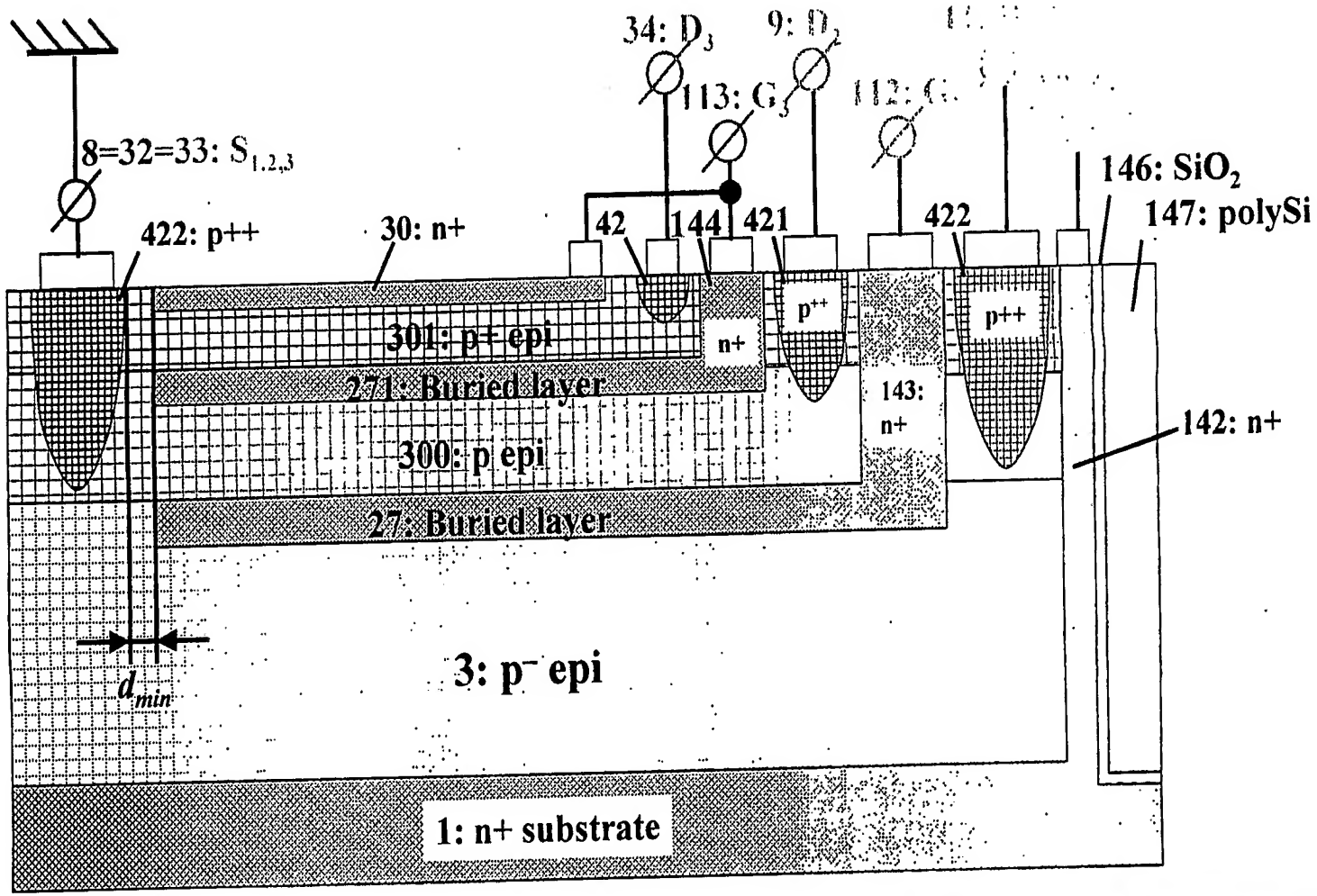


Fig.42-b: A.3) Triple JFET (bulk AND surface channels) imaging device
b.3) Separate channels and common source



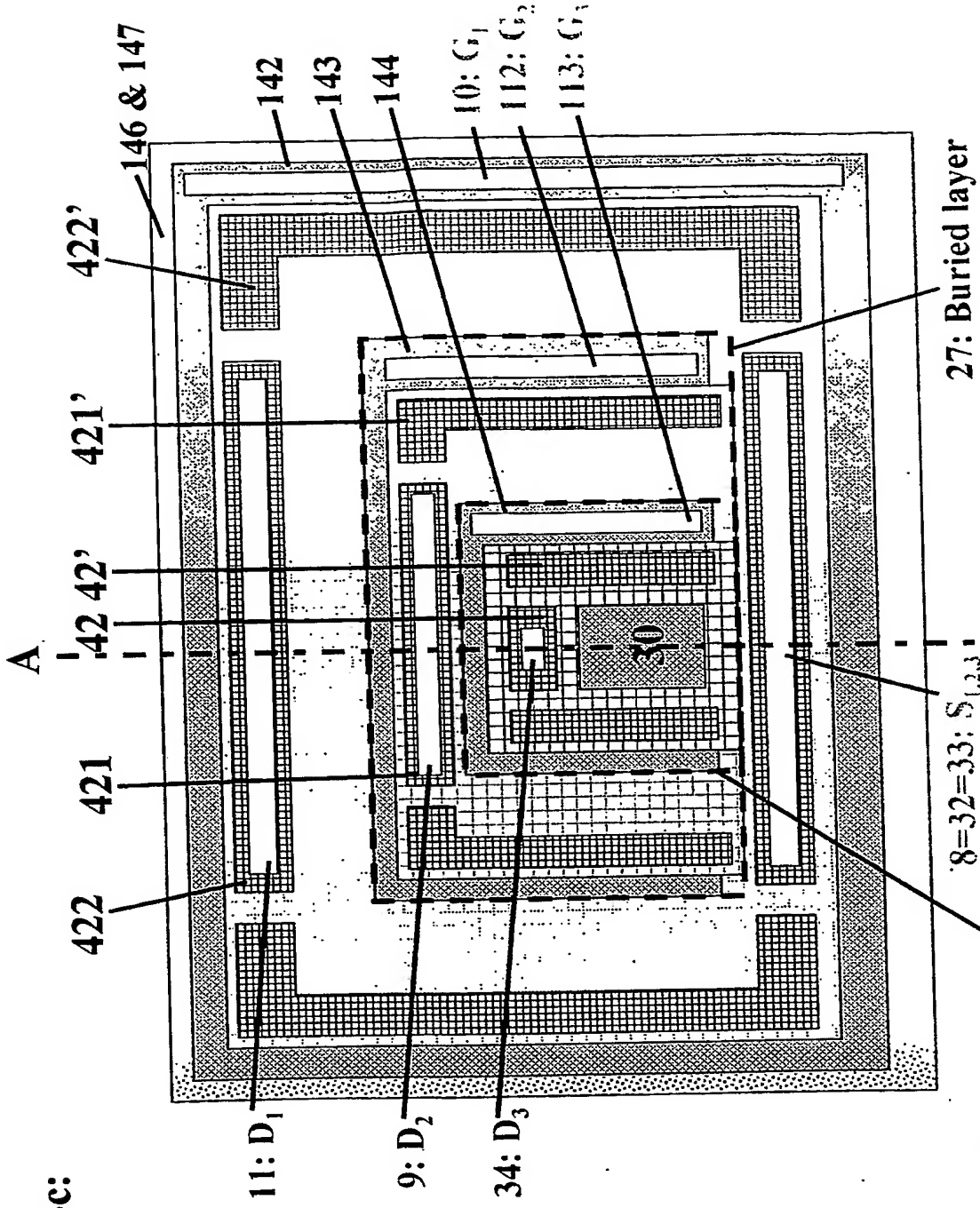
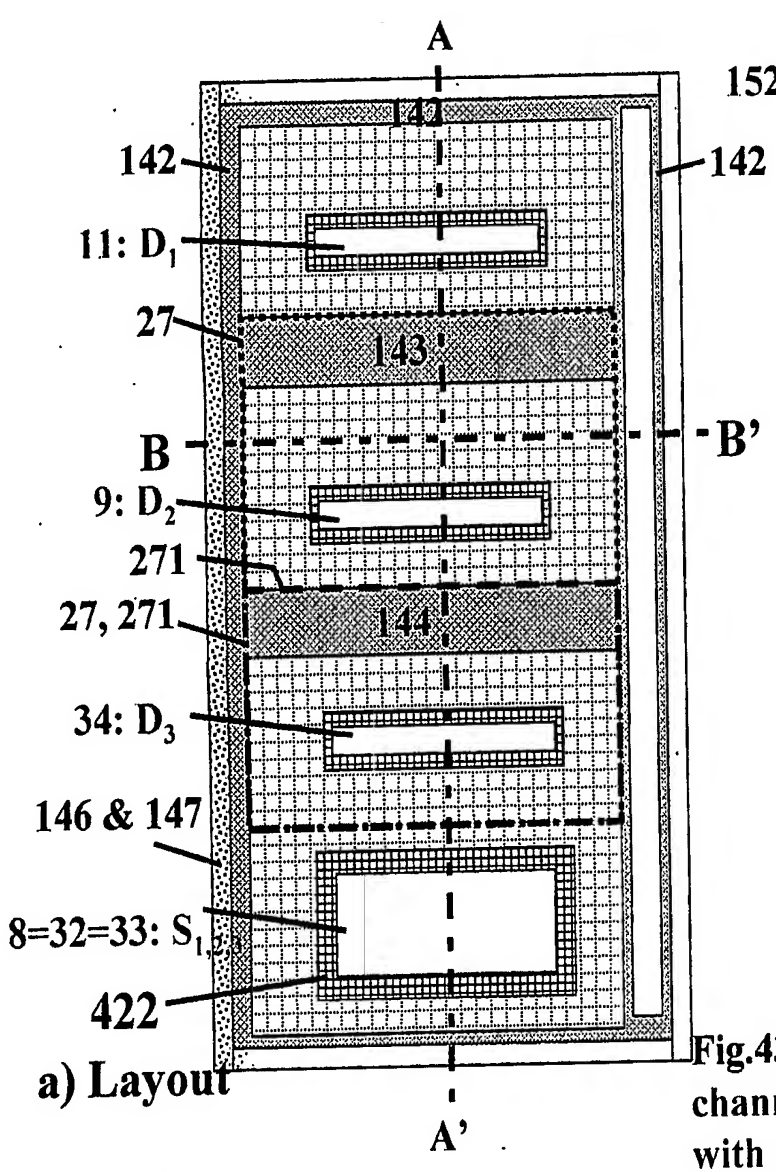
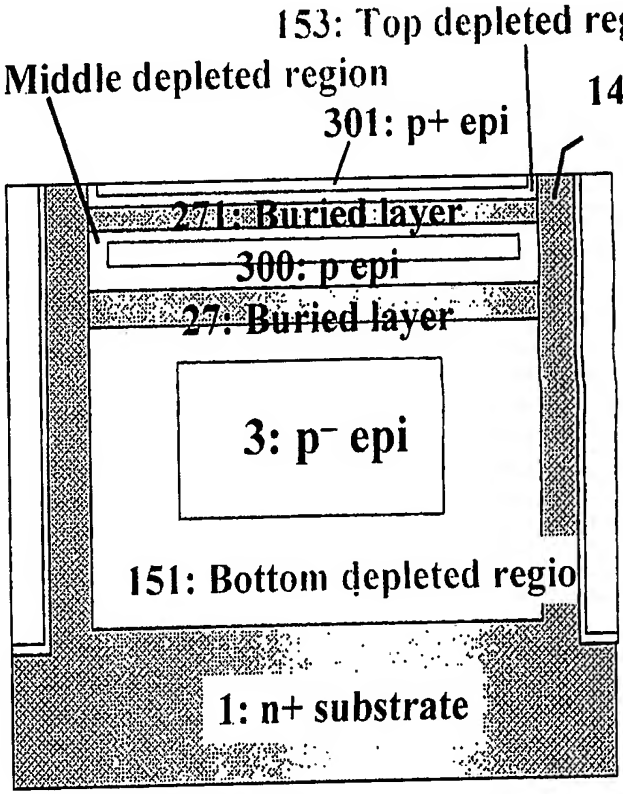


Fig.42-c:





b) B-B' cross-section

A-A' cross-section=
identical with Fig.42-b:

Fig.43: A.3) Triple JFET (bulk AND surface channels) imaging device: b.4) Separate channels with common source & common gate

B) FCT-based (***vertical*** channel)

B.1) BULK channel

B.1.1) Basic structure (stand-alone device):

Fig.44:

a) Separate A & G

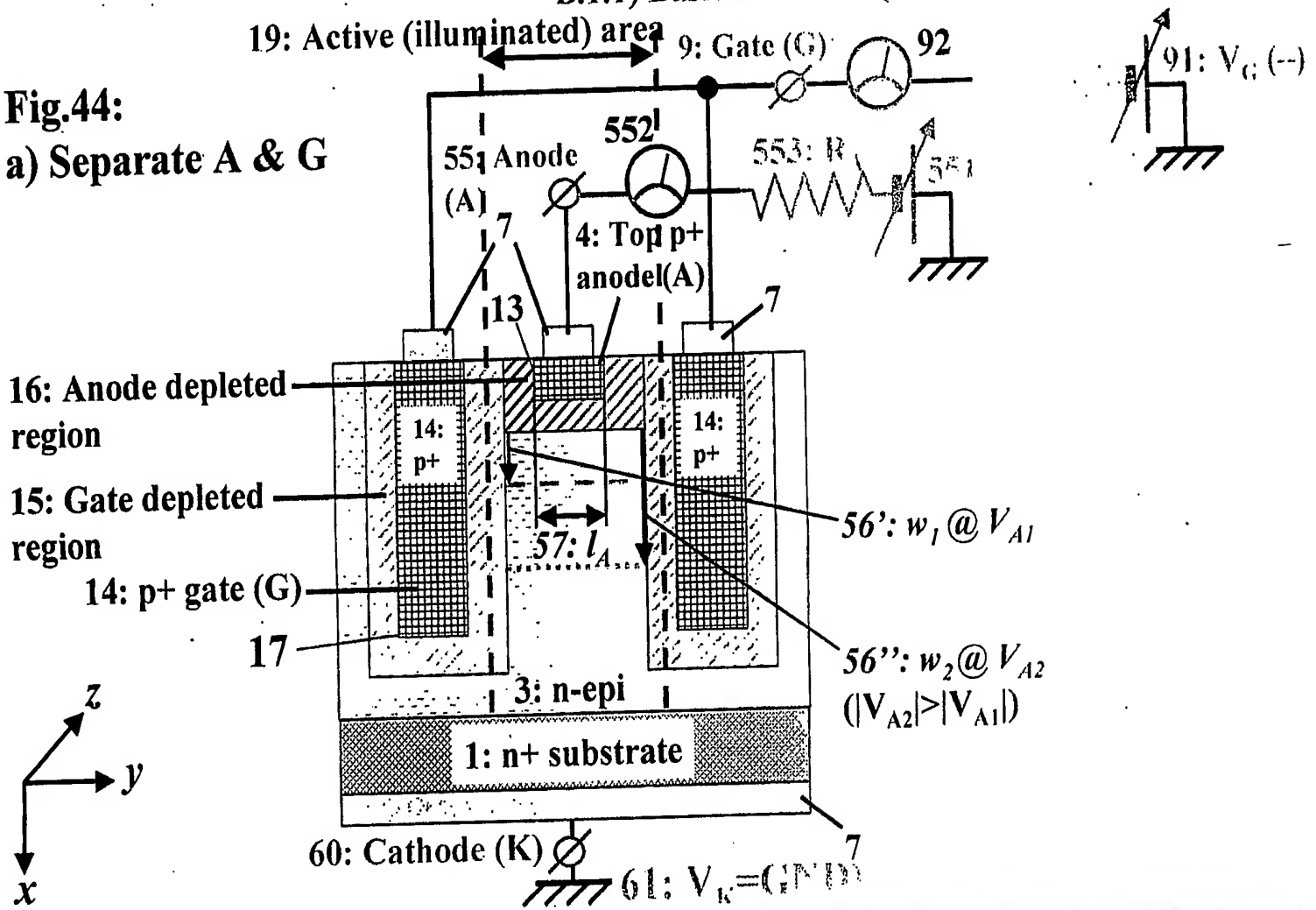


Fig.44:
b) With polySi-filled trenches

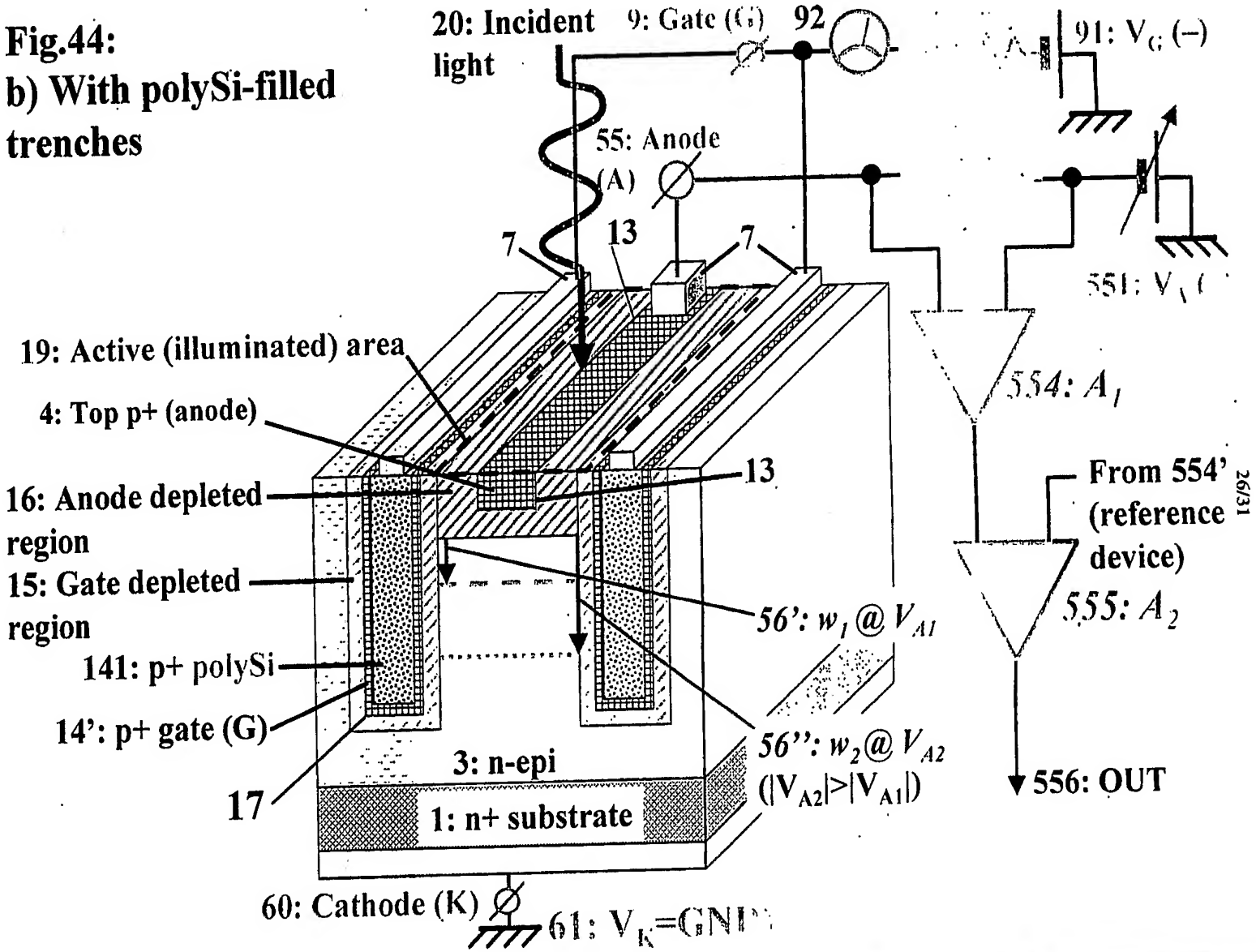


Fig.44:

c) Merged A&G

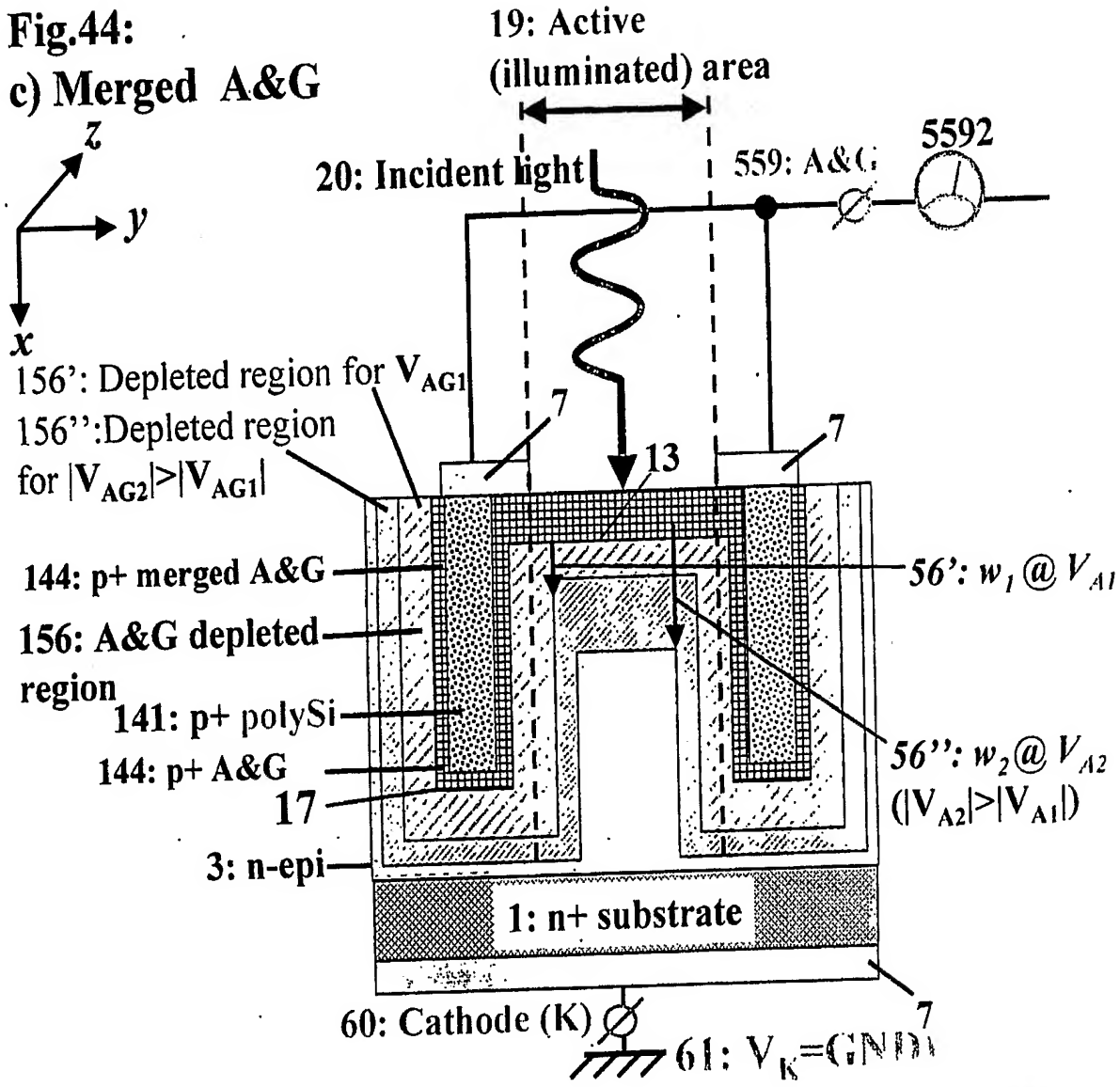
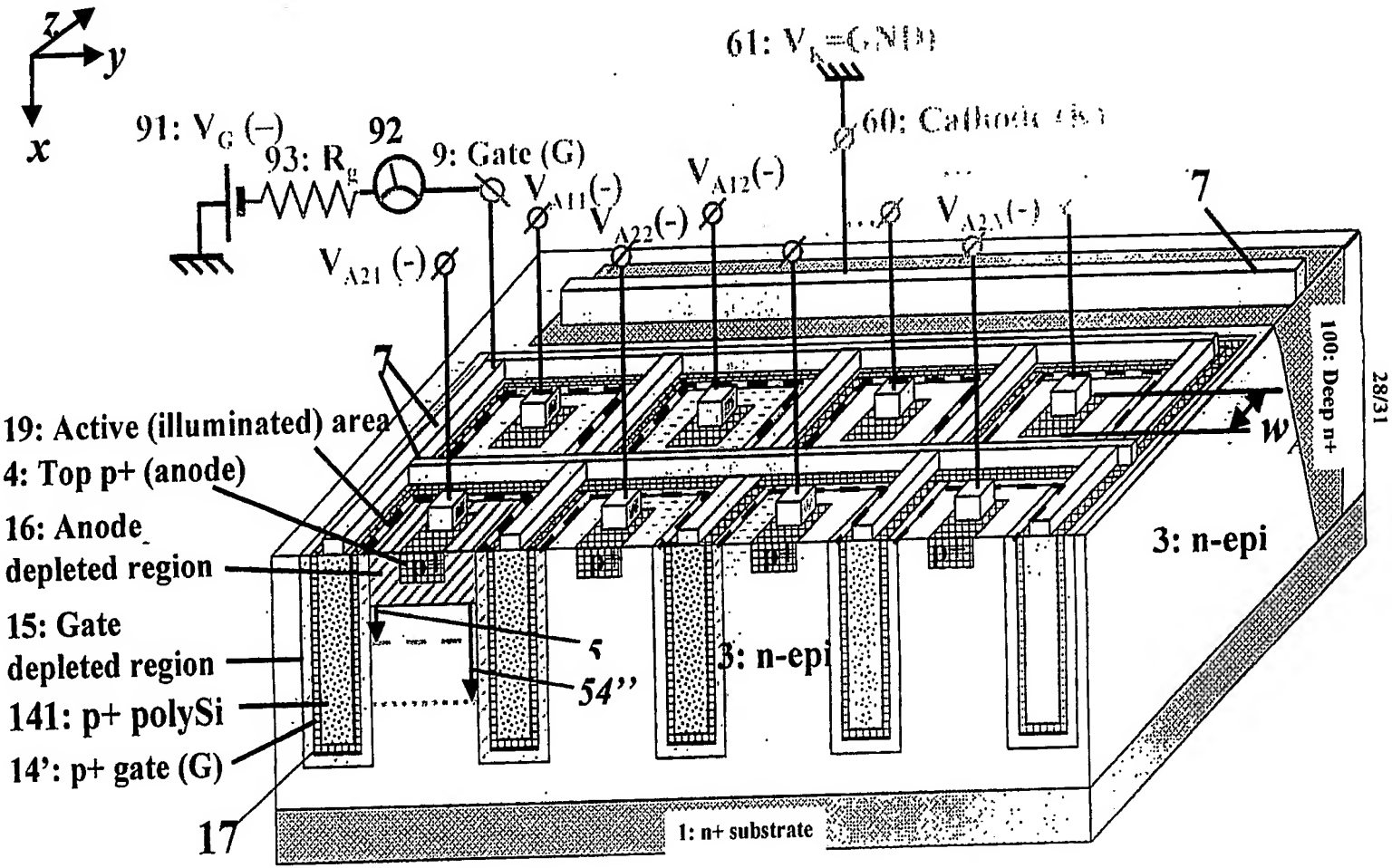


Fig.44-d: **B.1.2) FCT-based colour sensing array**



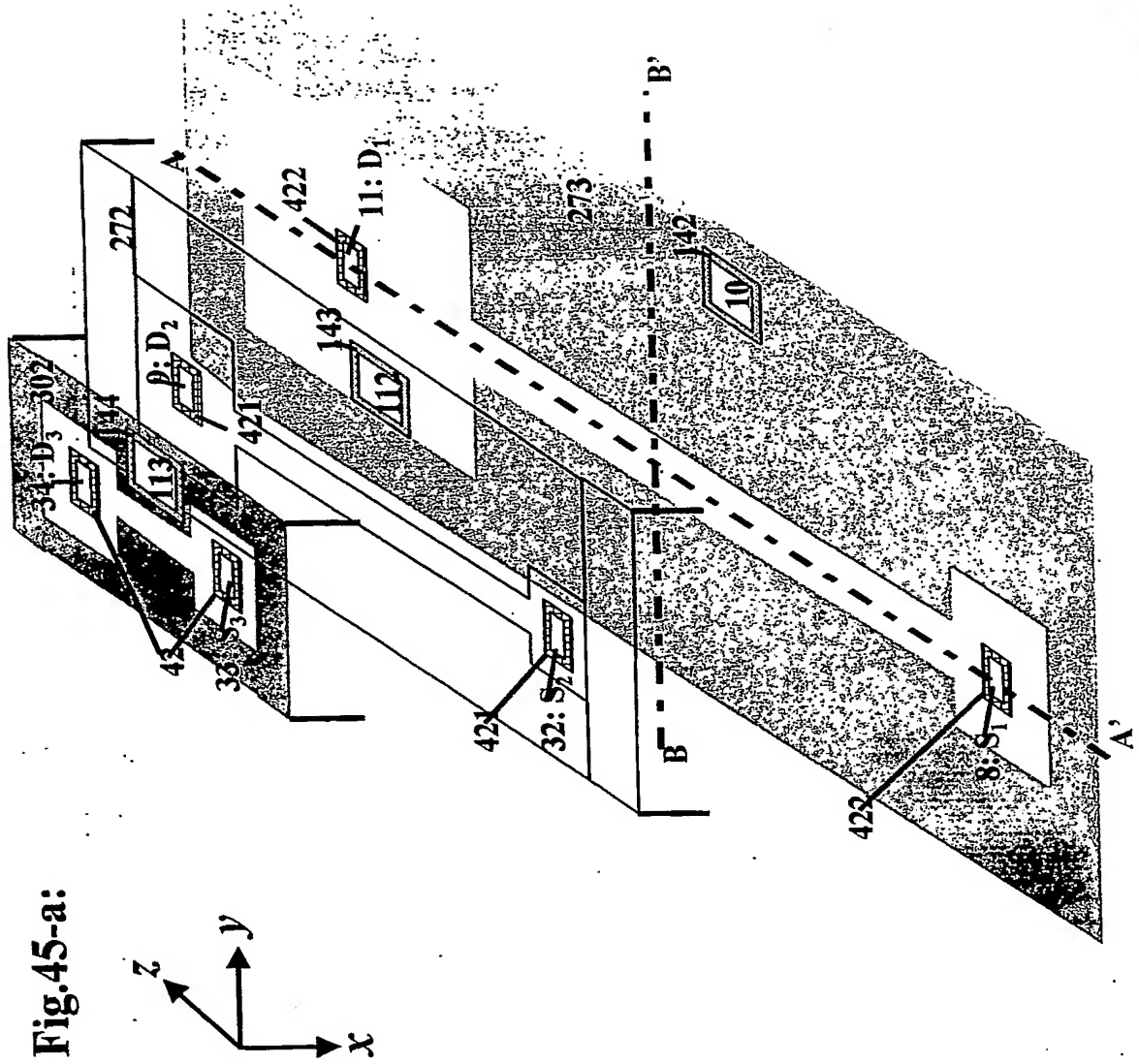


Fig.45-a:

Fig.45-b:

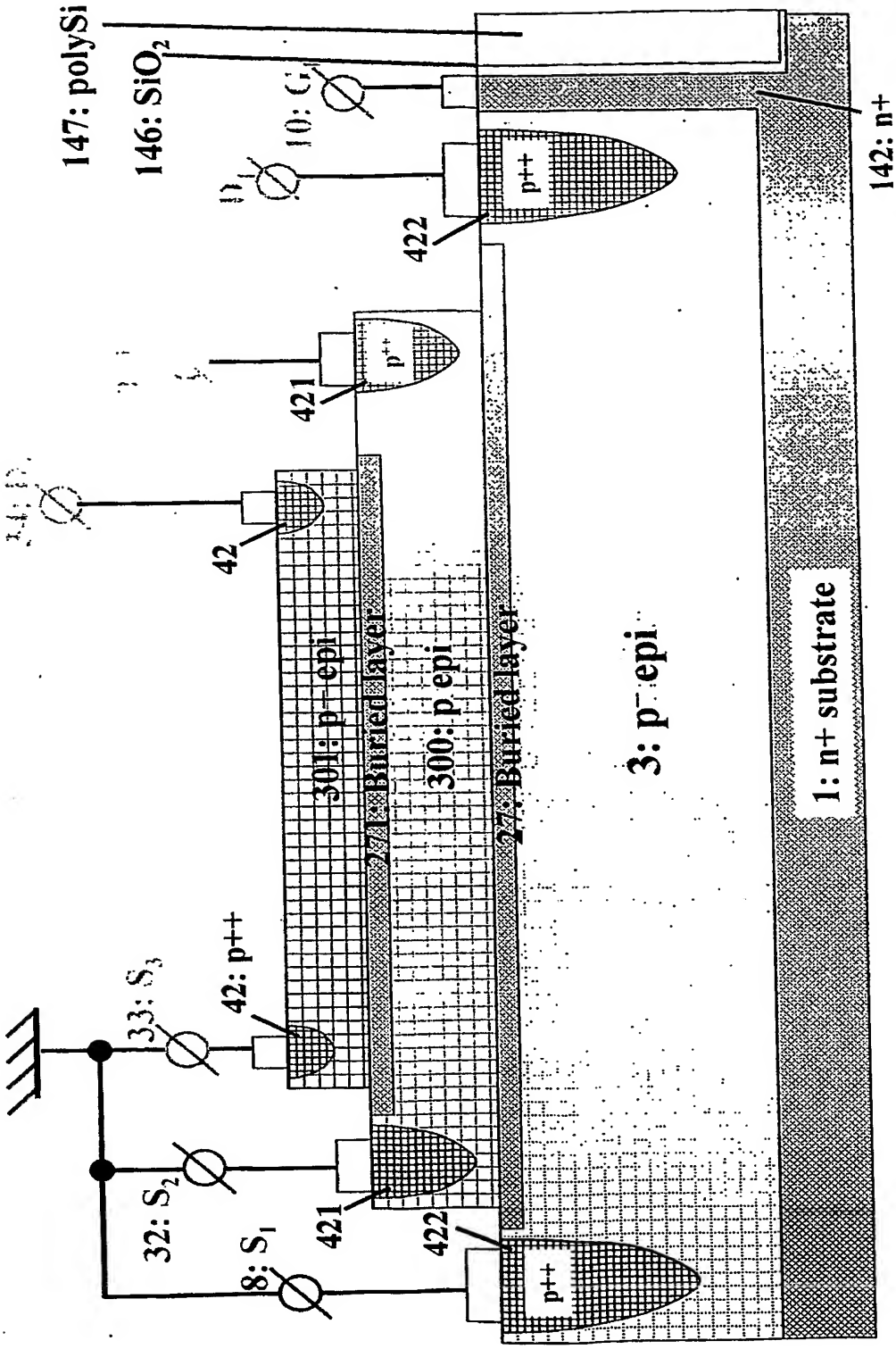


Fig.45-c: